

# Evatronix IP Enhances Competitive Advantage with a Little Help from 0-In Formal Verification

*Mentor Graphics® 0-In® Formal Verification improves the quality of Evatronix IP through exhaustive coverage, proven industry protocols and checkers, as well as support of assertion-based verification. Such thoroughly verified cores instill confidence that they will work in any customer's design environment. Confidence translates into everyone saving time and money.*

Since its foundation, Evatronix S.A., headquartered in Bielsko-Biala, Poland, has put a lot of effort into delivering IP cores of the best possible quality to help customers create innovative products in less time. In 1997, Evatronix' first commercial IP core, C8051, was designed as a pin replacement for the Intel™ 8051 chip and, therefore, had to comply exactly with the same high standards as the original component. Its adoption of the Reuse Methodology Manual in 1999 and code coverage tools in 2001 were clear confirmations of Evatronix' dedication to IP excellence.

As soon as the Property Specification Language (PSL) brought assertions to commercial design tools, Evatronix jumped

on the idea of introducing assertion-based verification (ABV) into their simulations to improve the observability and functional coverage of their IP under test. They became convinced that formal tools would further enhance these verification capabilities.

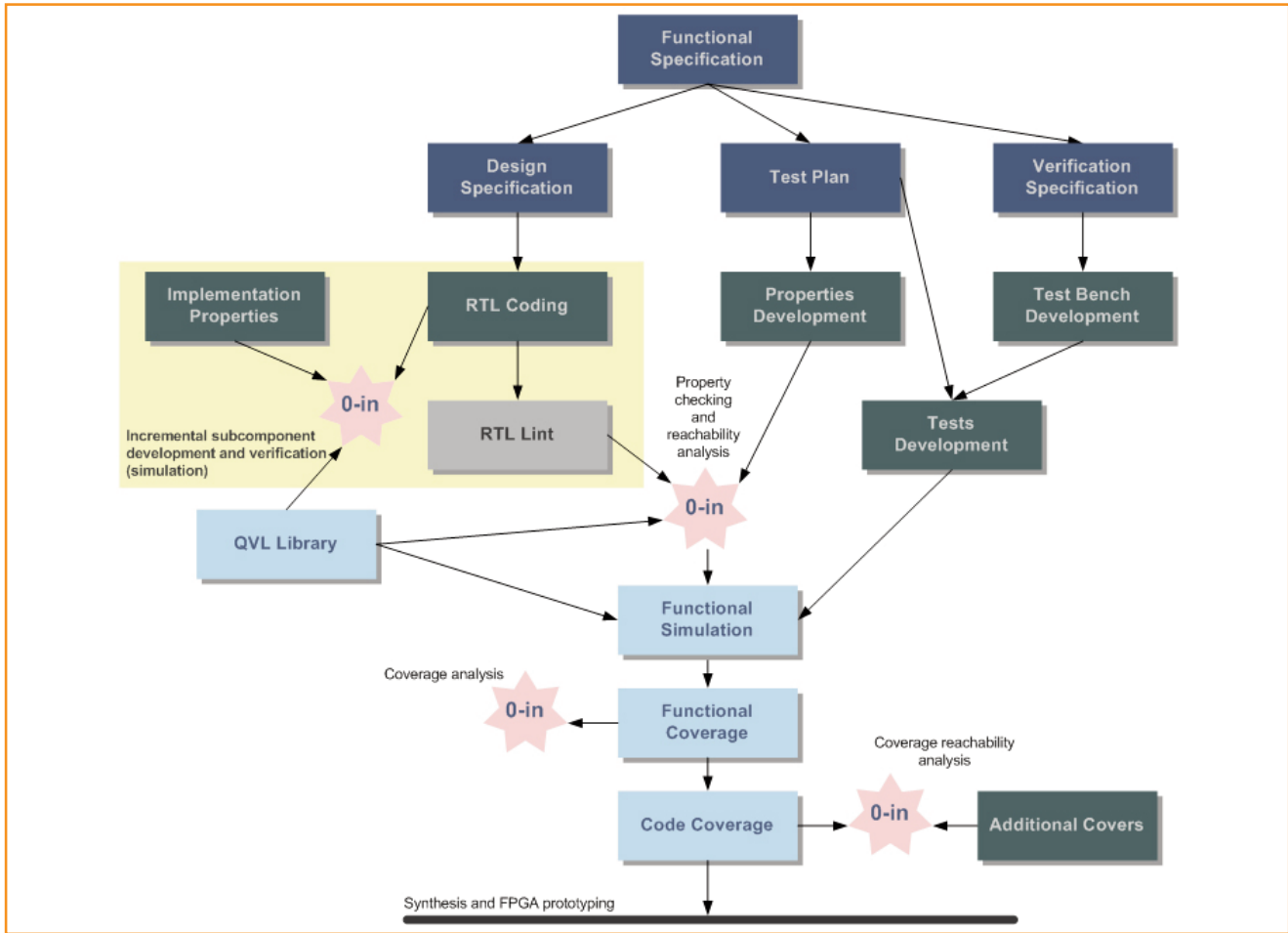
“We believe formal verification is a must for a company that is entirely devoted to providing the best IP solutions possible,” Wojciech Sakowski, President and Chief Strategy Officer of Evatronix explains. “Once we switched our work flow to assertion-based verification, we

“0-In Formal Verification cuts our time-to-market and increases overall product quality. The fact that our code is formally verified gives us a huge competitive advantage over other IP providers.”

**Wojciech Sakowski**  
President and  
Chief Strategy Officer  
Evatronix



*Ireneusz Sobanski and Wojciech Sakowski with the renowned ISO 9001 Quality Management System certificate of compliance.*



*0-In Formal Verification contributes a comprehensive methodology and complete solution to the Evatronic functional verification flow.*

needed tools to help us fully utilize that methodology, including the mix of languages inherent to IP use.”

### **Fixing on a Formal Solution**

Thus inspired, Evatronic started the search for the best formal tool for their design and verification flow. After evaluating several of these, they determined that the 0-In Formal Verification tool from Mentor

Graphics was the only tool that defused the state explosion issue and supplied an integrated, multi-language solution with simulation and assertion checkers and monitors. 0-In Formal Verification made it possible for them to improve the quality of their IP by enhancing their ABV methodology, which then resulted in increased customer confidence.

“0-In gave us more than just a formal engine,” Ireneusz

Sobanski, Verification Engineer at Evatronic reports. “It provided a very comprehensive methodology, including third-party checkers, and a really complete solution comprising everything from a fully static model checker to a unique dynamic formal engine. Thanks to such a holistic approach and its seamless integration with the Questa® simulator, we were able to take advantage of formal verification even in projects where formal

methods are hard to apply due to the state explosion problem.”

“Now we have 0-In, we consider formal verification as a much more simple and effective methodology,” Mr. Sobanski asserts. “Once time-consuming tasks, such as bus adaptation, now take about 10 times less time than they used to. Moreover, we do not need any testbench environment or tests to check the modifications – 0-In and the appropriate monitors, like AMBA™ or OCP™, are all we need. Of course, verification is only a part of the whole IP design process, but because we can now verify our IP better, we can deal with problems much earlier.”

## 2 + 2 = 5

In addition to the exhaustive coverage provided by dynamic formal verification, the other advantage the 0-In solution had over the competitors can be found in the Questa Verification Library (QVL). QVL enabled Evatronix to check an IP core’s functionality in the whole range of its applications and development environments. QVL provided a fast and easy compli-

ance checking solution and was particularly beneficial when there were no external tests available to verify the IP.

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**Verification Engineer**  
**Evatronix**

“Nobody else provides anything like the QVL,” Mr. Sobanski observes. “Mentor’s QVL library helps us check if a piece of IP would work in our customer’s SoC. By using the Mentor library, we can check our IP with external components to make sure it works correctly when integrated within the system. This feature benefits us

and our customers. Furthermore, QVL’s seamless integration with 0-In gives us more than enough scenarios to verify our work.”

## Flawless Code and Better Process

Thanks to the extensive testing methods provided by 0-In, Evatronix customers can take for granted that the IP they get will perform just as it’s expected to. This trust increased Evatronix’ competitiveness while reducing time-to-market and costs at the same time.

“0-In Formal Verification cuts our time-to-market and increases overall product quality, so we can concentrate more on developing new products or new value to existing ones,” says Mr. Sakowski. “Formal verification also gives us much more confidence when we take the product to the market. The fact that our code is formally verified, which is an exception rather than the rule, gives us a huge competitive advantage over other IP providers. Still, I hope all design houses will switch to formal verification in near future, as it just pays off.”

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