

DEVELOPING THE CONCEPT OF HARDWARE MODELING TO ENHANCE VERIFICATION PROCESS IN VIRTUAL COMPONENT DESIGN

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Abstract. *The role of hardware modeling in virtual component development process will be presented. Its influence on quality and verification time, technical solutions used so far and the new approach to this technique, developed to enhance the functionality and efficiency of hardware modeling.*

1 Introduction

Evatronix company specializes in design of advanced System-on-a-Chip components (*IP cores*). The final product in form of an HDL code arises as a result of a complex development process. The most important quality factors of the product are the faultlessness and the on-time delivery. Both of these factors are under significant influence of HDL code verification.

The solutions to be presented here correspond exactly to that stage of development process, with emphasis on their influence on efficiency growth and time reduction.

2 Virtual component development process

The VC development process consists of the following stages:

- Requirements determining and functional specification
- Test suite development
- Top level partitioning and HDL coding
- Subcomponent integration and verification (including prototyping)
- Productization

The productization stage covers the definition and realization of all deliverables: soft and firm version of cores, scripts for controlling different simulation, synthesis and FPGA Place-and-Route tools, Verilog version (translated from VHDL) and the User Guide.

3 Hardware modeling – a look in the past

By hardware modeling we mean the use of a real circuit as a model inside a simulated system (containing that circuit). E.g. we can build and test a virtual microprocessor system using the real microprocessor chip, leaving the whole environment (memories, application-indispensable hardware accelerators, Input/Output devices) inside the simulator.

At the turn of the 80'ies and 90'ies, hardware modeling was used in a board-level system simulation due to the lack of behavioral models of LSI/VLSI devices used in package construction. The CATS modeler built by Racal-Redac dates back to those times. Together with a SUN workstation and CADAT simulator they form a system that enables us to carry out the simulation of circuits consisting of physical components (ICs) without having their behavioral models (bus or fully functional).

4 The use of hardware modeling in VC development

Depending on the realized virtual component, hardware modeling may be useful during research and test development stage. The greatest role of hardware models comes with reverse engineering, when the goal is the recreation of the functionality of existing catalogue parts (usually obsolete), with various degree of accuracy in recreation of their original timing. Reverse engineering is essential within formation of the specification of the virtual component (VC) under development. Hardware models ensure the full (tick-to-tick) or just functional equivalency between our components and reference chips.

Hardware modeling resolves many ambiguities that pop up after referenced chip documentation. As an example of a design using reverse engineering we may name a microcontroller core compatible to the classic 8051 instruction set architecture and containing the same peripherals.

Hardware modeler is also useful for testing the FPGA prototypes of virtual components, independently on its use or not during specification stage.

5 Solutions used so far

The CATS-CADAT system referred to above has been used so far at Evatronix during test suite development and FPGA prototyping. It is a networked system consisting of a SUN workstation running CADAT simulator and the CATS hardware modeler.

The CADAT simulator works with behavioral models written in BMD (*Behavioral Model Description Language*), a C-like HDL. The user builds environmental models such as ROMs and RAMs, signal generators, models serving as logic analyzers and glue logic enabling the coexistence of all components. The physical device (e.g. a microprocessor) installed into CATS device (using a special cartridge) is connected to the simulated environment and can be treated as any other behavioral model.

6 The new approach to hardware modeling

The growth of requirements for hardware models comes as a consequence of developing more and more complex virtual components. This situation brings about problems of too many pins of the reference chip, system overload due to many simultaneous simulations, long-lasting preparation of a new model and lack of ability to model some physical features (e.g. bidirectional asynchronous pins). The fact that definition of simulation environment demands a skill in using an exotic BMD language and unusual simulation environment is also a severe restriction.

The solution to those problems is the new system currently being developed at Evatronix under the working name of “Personal Hardware Modeler” (PHM). This name describes accurately the basic assumption which is the transition from a centralized workstation to a desktop device to be connected to any PC class machine. From the user’s point of view the new system is to be at first as easy as possible, allowing the preparation of a new hardware model by any engineer not having any specialized knowledge on hardware modeling. The biggest effort is now reduced to the design and manufacturing of an adapter-board connecting the reference chip with the modeler.

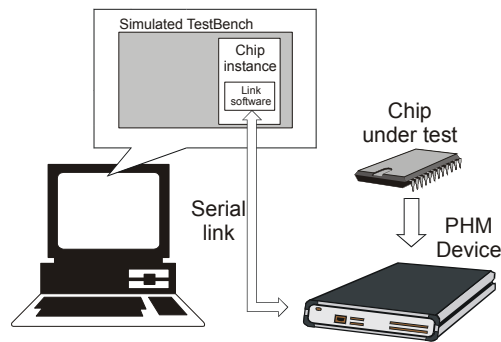


Figure 1: PHM system functional diagram.

The rule of operation of the modeler is similar to CATS system mentioned before. It is based on periodic stimulation of the reference chip followed by its response detection (it is called *dynamic modeling*). The PHM device is built upon an FPGA circuit containing serial communication interface to the PC and other logic that performs stimulation and response detection on a reference IC. PHM stores stimulation vectors in local memory, applies a sequence of them to all input pins of the device under test in real-time, and sends detected responses back to the PC, where they are processed by VHDL simulator.

The goal of a whole system is to substantially improve the reference circuit examination process, test suite development and VC prototype verification.

7 Advantages and disadvantages of both solutions

The most important advantages and disadvantages of CATS modeler and PHM system are shown in Table 1 and Table 2.

Table 1: Advantages and disadvantages of CATS modeler.

CATS modeler	
Advantages	Disadvantages
<ul style="list-style-type: none"> • Network interface and possible access from every point of a LAN • Possible work with multiple hardware models in a single environment, as well as with multiple simulation sessions run from different network places. 	<ul style="list-style-type: none"> • Limited number of pins, inability to work with bidirectional asynchronous pins • Simulation time limited to few milliseconds • Complicated maintenance, the need of experience during preparation of a new hardware model. • Works only with CADAT simulator. Two simulation test benches needed – VHDL and BMD (Behavioral Modeling Language). • Huge size, weight and power consumption making the device non-portable. • The risk of a master failure and eventual death of the 10 years old system. • Low performance (unable to use the system as a simulation hardware accelerator).

Table 2: Advantages and disadvantages of PHM system.

PHM system	
Advantages	Disadvantages
<ul style="list-style-type: none"> • Increased number of examined device pins (max. 150), freely configurable. • Huge simulation time possible (tens of milliseconds – 64MB of RAM used). • Device portability – small size, low power consumption, serial communication with a PC. • Compatibility with standard VHDL simulators, the same environment (Test Bench) for virtual component and hardware model simulation. • Possible use as simulation hardware accelerator for FPGA post-route verification. 	<ul style="list-style-type: none"> • Only a single hardware model may be simulated in one test bench. • The need of having a VHDL simulator compliant to Tcl, FLI or VHPI at a local computer.

8 Where the improvements are

The basic foundation of looking for the new approach to hardware modeling is to improve the performance to shorten reverse engineering, test suite development and prototyping stages of Virtual Component design. What comes as additional virtue is the integration of those stages with the use of single simulation environment.

The experiments comparing the PHM solution to the legacy CATS-CADAT system show that the goal will be reached.

The table below shows which elements of the system have been improved and what the profits are.

Table 3:Hardware modeling improvement areas.

Improvement area	Predicted profits
<ul style="list-style-type: none"> • New hardware model development 	<ul style="list-style-type: none"> • Time shortening from weeks to days
<ul style="list-style-type: none"> • Moving some operations from simulator to hardware, e.g. detecting of logically invalid state ('Z' or 'X' value) propagation 	<ul style="list-style-type: none"> • The number of vectors to be sent from hardware to simulator reduced twice • Simplified (therefore faster) software service of illegal signal values
<ul style="list-style-type: none"> • Design as a dedicated IC with simple interface to the host PC 	<ul style="list-style-type: none"> • Modeler response shortened to the minimum
<ul style="list-style-type: none"> • Moving the required simulator to a desktop PC (cheap and constantly improved) 	<ul style="list-style-type: none"> • Making the simulated test bench environment to work faster, making it practically unnoticeable in comparison to the hardware device and serial communication
<ul style="list-style-type: none"> • Limiting the transferred data only to the information about signal transitions 	<ul style="list-style-type: none"> • Lower data rate required

Figure 2 shows the comparison between CATS-CADAT and PHM systems. The time required to run the simulation is shown against the time of test procedure. This relation can be expressed as below:

$$T = n \times Tc + \sum_{i=1}^n i \times Th \quad (1)$$

where T means Run Time (as in Figure 2), n is the current number of simulation steps, Tc represents the time required to process the hardware model response at each simulation step, and Th is the time of hardware model resolution. The Th fraction brings nonlinearity to that formula, but that's where we cannot improve anything if we still want to talk about dynamic modeling. The Tc part of equation (1) represents the time required for sampling the reference chip response, transmitting it to host computer, processing by simulator and sending the results back to hardware. That's where PHM system shows the improvements.

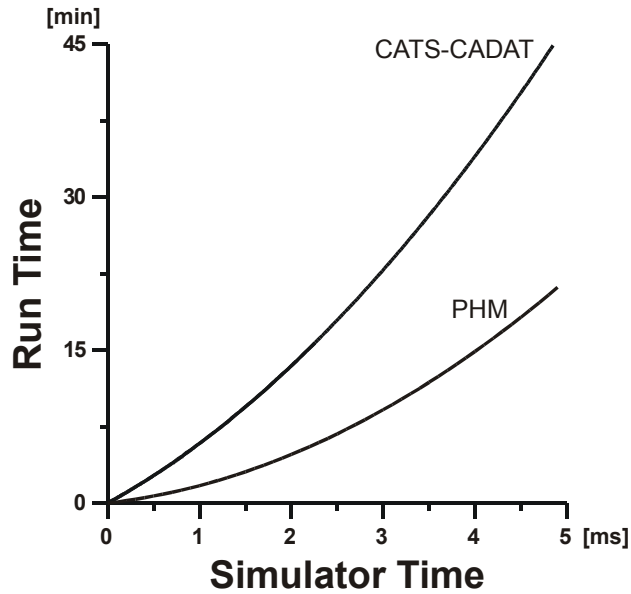


Figure 2: PHM vs. CATS-CADAT performance.

Those results were taken from 16-bit DSP hardware model working at 10MHz. As we can see the PHM improvements are significant especially when we realize that there are typically hundreds (or even thousands) of test simulations to be run during one design.

The typical VC design flow shown in Figure 3 points that stages connected with the use of hardware modeling are incorporated directly into the critical path. We can save about two weeks at new model development, another two weeks at test suite development stage and a few days at prototype testing, which makes the whole month in a one-year design.

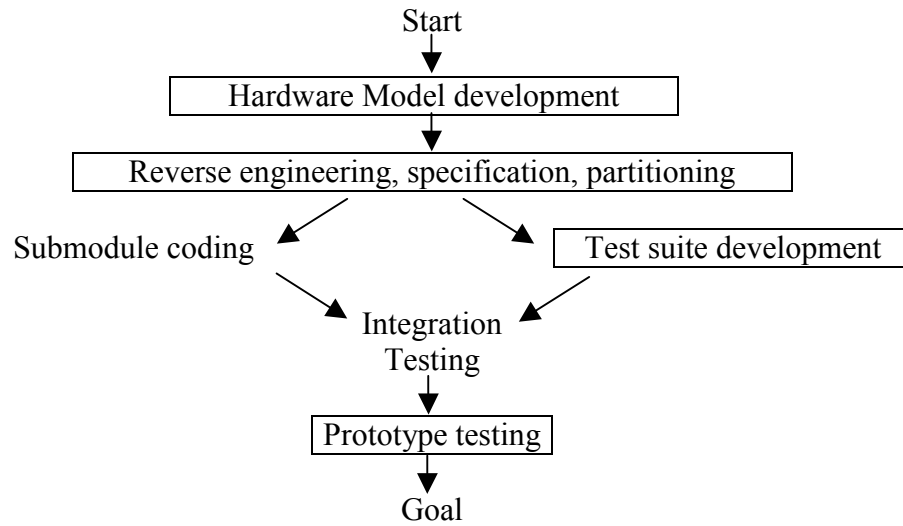


Figure 3: Typical VC design flow with stages dependent on HM highlighted.

9 Directions of development

- Connecting many PHM devices using a dedicated hub to allow multiple hardware models simulation in a single VHDL test bench
- Accelerating hardware operation: by setting some restrictions on examined circuit's architecture, static modeling (as opposed to dynamic modeling used so far) may be applied. It will significantly shorten the time needed to stimulate the reference chip and enable to emulate any hardware prototyped
- Speeding-up the interaction of the device with a simulator. The growth of software speed will allow the use of PHM as a hardware accelerator (emulator) for FPGA prototype post-route simulation
- Adding extra debugging features: The simulation may be partially re-started, allowing to modify a part of test procedure without re-simulating the part that wouldn't have changed.
- The integration of PHM system with debug circuits implemented inside microprocessors (e.g. the On-Chip Debug Support – OCDS – developed by Evatronix). After that, internal resources of the microprocessor will be visible for the simulator. This would work as a logic analyzer installed inside the processor.

10 Conclusions

The experiences from designs realized at Evatronix indicate the essential role of hardware modeling during virtual component development, especially those that require some reverse engineering. Efficiency requirements create the need for developing this verification technique towards fast devices that are simple in use and accessible for each designer. The use of FPGA in their construction allows to be up to the needs and opens wide prospects for further improvements. The current stage of development proves the PHM concept to be operational and confirms advantages of application of FPGAs to control dynamic hardware modeling.

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