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The Keynote from the President:
ECSI Achievements in Fall 2001

by Lars-Olov Eriksson

The annual Forum for Design Languages took place in the first week of September. This is a particularly dear event for ECSI and a natural opportunity to gather people for ECSI related events.
This time there was a one day ECSI-SYDIC meeting, a meeting to take a new initiative in the field of languages for systems specification and design and a meeting of the Executive Committee.

The ECSI-SYDIC meeting

In cooperation with the SYDIC-Telecom project the ECSI-SYDIC assembled, in addition to ordinary ECSI members gathering representatives of the automotive industry and invited participants from VSIA and Accellera. As part of the prepared program recent achievements and current status of all projects under ECSI care were highlighted. Dave Barton from Accellera presented their two main activities of interest to ECSI as a partner: the Semantics group and the Rosetta group. Gjalt de Jong from Telelogic presented their view of the future of UML, including new OMG initiatives, as a systems specification language and outlined their ambitions regarding UML2.0/SDL2000, a suggested new part of the core of standard UML.
Finally opportunities for a deeper cooperation between ECSI and VSIA on systems level design methodology were discussed.

The SYDIC-Telecom project

The current status of SYDIC-Telecom was presented in an overview given by Jean Mermet. Based on the evaluation of the project by the Commission in March and recommendations following, the project has adjusted its direction and its strategy - most noteworthy is a concentration of the resources available on the core issues.
Mermet explained and described how the project had proceeded to make the necessary adaptations and which are now the key activities of the project. One result of the adjustments made is the clear focus on reuse - as a concept and as a practice - in one separate activity.
Konstantina Barkoula from Intracom, responsible of this particular work package, presented a first cut at an inventory and at a classification system, further highlighted different strategies for reuse.
Key in the project is the establishment of a conceptual model for systems under design and for the design process as a base for the analysis of reuse and systems specification practice. This model is evolving throughout the project. Still preliminary a more mature version is planned to be ready in the beginning of next year. Dissemination of results being an important part of the mission of the project, this model would be a natural subject for ECSI-SYDIC. Most notably the notion of a common ground for exchange of views between the telecom and the automotive industries is a very appealing one.

The ODETTE project

ODETTE is another project running, engaging some of the ECSI members, where ECSI is doing efforts related to dissemination and standardisation but not to management. It is aiming at a SoC design methodology developed using object oriented paradigms extending the SystemC language.

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ECSI Achievements in Fall 2001

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Expected results encompass the standard object oriented extension to SystemC as well as consistent the consistent design flow and tool support. The project is currently approaching the phase of first prototypes validation.

The SYDIC-Automotive project

For quite some time now ECSI has made every endeavour to include the automotive industry in the ECSI enterprise.
Encouraged by initial experience with an ECSI-SYDIC meeting, addressing the automotive industry, in June 2000, an ECSI initiative has been taken and pursued in several successive meetings.
In an attempt to collect forces in the automotive industry a project has been outlined, aiming at the solving of some of the systems design problems of that industry.
Shaped after the pattern of the pioneering SYDIC-Telecom project, ECSI and SYDIC-Telecom partners would assist in the forming and launching of a SYDIC-Automotive consortium.
On behalf of the Executive Committee Ian Phillips from ARM, the current chairman of the Technical Steering Committee, has carried the responsibility and shared the main effort with Adam Morawiec from ECSI staff in this undertaking.
At the ECSI-SYDIC meeting Ian Phillips reported on the progress that had been made with nine participating car manufacturers. The impression is that there is a lot of common issues and similarities with the telecom domain and indeed reason for the companies to do something about the challenges.
It is now up to the automotive partners to consider the findings and take the opportunities offered to make the project happen.

Other projects under preparation

Preparations are ongoing for a project on education, ECSI-Training, the idea being that ECSI members together with centers of excellence would define and organize advanced education for experienced designers and design managers. The application recently was submitted.
In an initiative originating outside ECSI, called SystemC in Europe, the intent is to collect and assemble requirements on and practically evaluate results from the development of SystemC. ECSI as such is considering participation together with some of its members. The application recently was submitted.
Internet-Based Intellectual-Property-blocks Distribution for Electronic systeMs design (IBIDEM) is a project aiming at a design and delivery methodology and a business model for IP reuse. The application recently was submitted.

The forming of a System Specification and Design Languages group

ECSI kicked off a new special interest group during the FDL week, the System Specification and Design Languages group. Launched to implement part of the ECSI strategy, i.e. to promote development of this subject, the group also serves a particular purpose. Thus, it is meant to be a means of communication for the Working Group on systems specification languages in the SYDIC-Telecom project: for dissemination of project results and for feedback from external expertise on the viability of propositions made. The project being in principle devoted to the problems, this group would be seeking solutions. The group is set to attract world wide participation.
Invited and present at the meeting were representatives of VSIA, of Accellera, of SYDIC-Telecom and of ECSI, in addition of independent expertise. Being supportive of the idea at large, the group made a first cut at an analysis of problems and opportunities and exchanged views of matters of concern and working modes possible.
The group being started in an informal way, the intention is to steam up the activity beginning with next DATE event. In the meantime the discussion will continue by e-mail and a reflector will be set up in order to facilitate communication among the members of the group.

The VSI Alliance

A stronger cooperation with VSIA will be ensured by the new agreement between ECSI and VSIA that is currently to be finalized shortly. This agreement will enable ECSI to directly provide VSIA specifications to the European companies and create special offers to the ECSI members.

The ECSI Executive meeting

In the Executive meeting a lot of matters due were handled, including various aspects of all activities going on or being planned. Two issues deserve particular mentioning.
The development of the membership is continuously followed and systematically watched by the Committee. The trend having been reported markedly changed to the positive at last General Assembly meeting, we were now pleased to notice a continued optimistic outlook on the future.
Based on experience with the SYDIC-Telecom project, some of which reason for concern, the Committee has set down criteria and rules for so called ECSI projects. We now went on to do the same for other projects in which ECSI may participate. This will add to the fundament of principles for ECSI which may be studied by any member in the so called Handbook.

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MEMBER PROFILE: EVATRONIX SA

COMPANY PROFILE

Evatronix S.A. was established in 1991 in Bielsko Bia3a and since then has been a value added reseller of PC-based CAD & EDA systems.

In 1997 company started development of **electronic virtual components**. This activity grew dynamically over last few years and in this year (2001) has become the main profit source for the company. Recently it has been complemented with extensive offering of electronic design services.

EVATRONIX MISSIONS

Company missions (that reflect its historic evolution) are as follows:

- to enable our customers to shorten time-to-market with innovative electronic products by offering them virtual electronic components (for use in system-on-chip designs) and by supporting them with design services,
- to stimulate adoption of computer-based design technologies by Polish industry.

BACKGROUND

Company was founded by W3odzimierz Wrona and Wojtek Sakowski who have managed it since its foundation. The professional background of the company founders is electronic design automation. They both graduated in electronic engineering from Silesian Technical University in Gliwice (Poland) in 1980, where they also got their Ph.D. degrees in 1990.

W. Sakowski worked at the Joseph Fourier University in Grenoble (France) within a framework of European CAD Integration Project (ESPRIT 2072) in 1992 and 1993. As a manager of VHDL Standardization Logistics Team he was a founding member of ECSI in April 1993.

From 1995 to 1998 W.Sakowski managed an EU-funded PHARE Project: TEMPUS S_JEP – 09151 – 95.

This project aimed at improvement of education in the area of modern electronic design methodologies at Silesian Technical University in Gliwice. Its success made available graduates well trained in HDL-based design, that did internships at EU companies. Some of them became Evatronix employees.

ACTIVITY LINES:

Virtual Component development

Up to now the company focused on development of commodity IP cores, revitalizing industry standard architectures for use in system-on-chip design. Current product line includes:

- Three versions of 8-bit microcontroller core based on Intel® 8051 architecture: C8051, D80530, R8051 & R80515; the latter executes one byte instructions within one clock cycle at clock rates of 100 MHz (for 0,25 mm process),
- C165x, C1655x - low cost microcontroller cores compatible with Microchip PIC® 16C5xx devices,
- CZ80cpu core and accompanying peripheral cores,
- 16-bit processor core code compatible with Motorola® 68000 cpu,
- digital signal processor core C32025 (code compatible with TMS320C25),
- serial transmission protocol controllers implementing I2C, SDLC & USB standards,
- numeric coprocessor compatible with Intel® 80187 device,
- C80186 (compatible with Intel® 80186 microcontroller, av. Q1'2002).

As company grows more complex projects are undertaken to shift the focus of developments towards more differentiating IP cores (star IP).

Electronic design services

This activity covers the following areas:

- On demand development IP cores & HDL simulation models,
- design of FPGA circuits for Xilinx and Altera technologies,
- embedded systems development (software and hardware, for variety of underlying processor architectures).

EDA & CAD system integration

On the Polish market Evatronix is known as a distributor of EDA solutions from Altium (Australia) and an Autodesk Authorized Dealer offering CAD systems for mechanical engineering.

QUALITY ASSURANCE POLICY

In order to ensure high quality of our products and its compliance to reference architectures a rigorous development methodology is applied.

HDL models are tested against reference chips by means of a hardware modeller. Test suit quality is measured by the code coverage tools from TransEDA.

Reuse Methodology Manual guidelines (by Synopsys and Mentor Graphics) are followed throughout the development process ensuring four star OpenMORE rating for most of the cores.

All cores are prototyped in FPGA. Evaluation is possible through encrypted simulation model or encrypted netlist for FPGA prototyping.

Many of the Evatronix cores has been introduced into the third part IP programs run by Altera (AMPP) and Xilinx (AllianceCore).

MARKETS SERVED

Activities in the field of IP cores and electronic design services are offered worldwide. Our customers and licensees include such companies as:

- ASIC design houses and fabless silicon vendors (e.g. obsolete part, FPGA conversion services)
- ASIC manufacturers,
- electronic system manufacturers (industrial control devices).

Among company European customers we may found renowned representatives from all categories mentioned above. However, most of the revenue is generated in Taiwan and USA. As ECSI associate member we intend to increase our presence in the European market.
EDA & CAD related operations address domestic market only.

EMPLOYMENT

Design department employs now twenty four full-time developers as well as four external consultants.

LOCATION & CONTACT

Evatronix headquarters is located in Bielsko-Biala and main development centre is located in Gliwice. Both towns are within one and one and half hours drive from international airports in Katowice and Krakow (both have daily connections to Frankfurt and other European airports).
Our products are available in most countries through the network of distributors of our American partner – CAST, Inc. (http://www.cast-inc.com).
This network includes ProDesign (www.prodesigncad.de) in Germany and Answer Systems (http://www.answer-systems.fr) in France.
Design services are available directly from Evatronix. For details please refer to the company website at:
http://www.evatronix.pl
or contact **Evatronix SA**, R&D Department, phone: +48 32 231 11 71, Fax: +48 32 231 30 27, e-mail: ipcenter@evatronix.com.pl

ECSI announces the creation of the System Specification and Design Languages Group

Lyon, September 4th, 2001

by Patrizia Cavalloro, Italtel

The first meeting of the newly created ECSI group on System Specification and Design languages took place in Lyon, France on September 4th, 2001.

ECSI has felt the necessity to have a language group for several months not only to give a voice to the European specialists, but also to create a link with the « SYDIC » projects (Telecom today, Automotive tomorrow).
The main goal of this group is to characterize existing formalisms against system specification and design requirements, and to chose a common semantics representation in order to clarify how basic concepts belong to the different formalisms.

Jean Mermet opened the meeting by welcoming the presents. The participants introduced themselves briefly.

The proposed agenda was approved. Jean Mermet, acting chair of the SSDL group, presented some slides with the goal to clarify the mission of the SSDL group, to identify the relation with existing related works and to organize the work.

The Mission

- The SSDL Group works on the identification of the concepts used to specify predominantly electronic systems and analyses the constructs of specification and design languages necessary to support these concepts

- The SSDL group cooperates with the Accelera semantics group to produce a meta-model representing these abstract concepts and there relations

- The SSDL group collects worldwide related works and feeds its results back to standardization bodies

The Strategy

The strategy that the group has identified in order to fulfill the mission can be summarized as follows, by:

- Characterization of selected languages /formalisms against the set of abstract concepts

- Identification of the different families of languages (typology)

- Selection of one or two major representative in each family

- Study of the coverage of the specification phase and of the design flow by each language or combination of languages

- Definition of requirements and foundation of a system architecture language

- Tentative redefinition of models of a system in different languages/formalisms as different views derived from a common meta-model

Means and Measures

The way the SSDL group is going to operate in order to complete its mission

- Convening the best specialists in Europe from academy or industry
- Initiating and conducting projects as a way to accomplish the goals, e.g. demonstration of concepts
- Seeking visibility and acknowledged competence, to achieve broad recognition among electronic systems users and designers

- Establishing a meeting place between the software and the hardware design cultures

- Establishing a meeting place between all industry domains of system design

- Co-operating with standardization bodies

Patrizia Cavalloro, SSDL group Secretary and responsible in the SYDIC-Telecom project for System specification languages, presented the SYDIC-Telecom Workpackage 4 “System Level Languages”: its goals, activities and results up to now. Being a relatively small project, SYDIC-Telecom needs external expertise to provide soundness to its work on this topic, and the SSDL group is for sure the best place where to find it.

Dave Barton presented the current status of the Accellera semantic group and the Rosetta group, and links with the SSDL group activities have been identified. ECSI will ensure that the work of the SSDL group will be worldwide, not only European

The SSDL group work will continue by e-mail, and next group meetings will be organized in conjunction with international events (e.g. DATE & DAC) as fringe meetings.

A reflector will be set up in order to ease the communication process among the members of the group.

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VSIA IP/VC Quality Development Group
First Meeting In Europe

by Pierre Bricaud, Mentor Graphics,
pierre_bricaud@mentor.com

I don't think that I need to introduce VSIA and remind you that ECSI is VSIA's European arm. The interesting topic is how two very strong groups, one driven by Mentor Graphics & Synopsys (RMM-OpenMORE) and the other by VSIA as a VC Quality Group, arrived to the conclusion that they should merge and pursue the activity under VSIA leadership but keeping Mentor/Synopsys participation. This is what happened at DAC 2001.

Let's backtrack somewhat. I remember very well the first alert from Gary Smith in his article in Virtual Chip Design of May 1997: The Revolution Isn't Coming-It's Already Here. At that time I was Worldwide Marketing Director for Compass Design Automation Front-end software tools and we were introducing the first stand alone RTL floorplanner: Design VP (Virtual Prototyper). In this article the discussion of design gap appears, as do the notions of system level integration (SLI) and system level macros (SLM). I will quote Gary: '*Another misconception about standards is that SLM design is as easy as fitting Lego's together. Nothing is further from the truth. Without standards, gluing these macros together is almost impossible. ASIC companies participating in this market have established their proprietary standards. The lack of Open Standards is preventing the use of mix and match SLM design even when we solve the silicon-specific problems.*' End of quote. Gary Smith was visionary in this article. As of today, the industry is still struggling for IP/VC Open Standards.

Let's start with OpenMORE. Everything begins when the hot topic was IP Reuse. After the first generation of early adopters, then the classical fall into the Chasm, the second generation of reusable IP in the 1999-2000 time frame began to reflect the expected productivity enhancements. A critical difference appeared and that was the notion of IP Infrastructure. The infrastructure covered many areas from legal to business practices to file formats and test benches. More importantly, there was a common acknowledgement from IP providers and IP buyers that a common infrastructure is required to streamline both the IP evaluation and the IP integration stages. The OpenMORE assessment program was an important component of the technical infrastructure.

The OpenMORE assessment program is based on the Reuse Methodology Manual (RMM), jointly authored by Mentor Graphics and Synopsys. It includes the complete set of rules and guidelines from the Synopsys MORE program, which was based on the original RMM. The last version of the OpenMORE assessment program is based on RMM version 2 and the hard IP deliverables document from VSIA. This was the first step towards the merger. OpenMORE with approximately 150 rules and guidelines for soft cores and nearly 90 rules and guidelines for hard cores provides the industry's premier methodology to simply and quickly evaluate the reusability of IP cores for SoC design. More than 45 IP providers and 100 cores were available in the IP catalyst catalog before the donation.

In parallel the VSIA board identified VC quality as a key industry concern. In September 1999 a Quality Study Group was created. A very important step was taken and that was the definition of the word Quality. Quote: 'Quality is a measurable conformance to customer or provider specified requirements.' End quote. During that period it was decided not to inject Quality into other DWG specs therefore opening the door to the specification of a quality attribute spreadsheet. A quality workshop took place in San Jose, CA, September 21-2, 2000. During that workshop a very important decision was made in a sense that it was recognized that quality had multiple axes. Four were defined: Authoring, VC Verification, VC Maturity, and Vendor Capability. The result of this highly effective work gave birth to the VC Quality Metrics spreadsheet version 0.6.

Now the real challenge lies be-fore us. Merge thoughts of two differ-ent origins and create an IP/VC Quality Metrics acceptable by all branches of the IC electronic companies. Danger is obviously to drown ourselves in definitions and specifications. It is my firm intention to drive the VC Quality DWG to success therefore providing the industry with an acceptable VC Quality Metrics spreadsheet. How? By blending the strengths of both groups, IP providers and System/SC companies, trying to focus on obtainable short term objectives and first of them being not to loose the valuable data that was gathered from the OpenMORE rating sheet. Then by using real cores, start the migration towards the more general VC Quality Metrics.

Again our goal is to deliver at DAC2002, Do or Die. I hope to see you before as a DWG member if possi-ble or at least requesting to be put on the mailing list of DWG results or at DAC 2002.

More information:
Pierre Bricaud: pierre_bricaud@mentor.com
or www.vsi.org

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Development of the OpenMORE Design Reuse Measurement Tool

The intellectual property (IP) industry is moving into its second generation of reusable IP and is beginning to reflect a maturity of business and technology that will drive IP to become the productivity enhancement everyone expects. One of the critical differences between today and two years ago is the growth of the IP infrastructure. The infrastructure covers many areas from legal and business practices to file formats and test benches. More importantly, there is a common realization from the IP providers and IP buyers that a common infrastructure is required to streamline both the IP evaluation and the IP integration stages. The OpenMORE assessment program jointly developed by Mentor Graphics Corporation and Synopsys, Inc. is an important component of the technical infrastructure.

Leadership in Design Reuse

Synopsys and Mentor Graphics have joined forces to help make IP reuse a reality. In June 1999, at the Design Automation Conference, Mentor Graphics and Synopsys announced plans for the OpenMORE assessment program, a free, Web-based measurement tool that can be downloaded by anyone at no charge. (See press release: Mentor Graphics and Synopsys Announce OpenMORE Assessment Program for System-On-Chip Design Reuse and Verification, June 20, 1999.) Open-MORE enables more rapid adoption of the best IP design reuse practices for system-on-chip (SoC) design and helps IP customers evaluate the reusability of the IP they acquire. The OpenMORE assessment program is based on the Reuse Methodology Manual (RMM), jointly authored by Mentor and Synopsys. It includes the complete set of rules and guidelines from the Synopsys MORE program, which was itself based on the original RMM; the recently released RMM Second Edition; and hard IP deliverables from the Virtual Socket Interface Alliance (VSIA) industry group specifications. OpenMORE was released at the IP99 Europe SoC Conference, November, 1999.

The RMM was co-authored by Pierre Bricaud, director of the IP Factory of Mentor Graphics, and Michael Keating, vice president of Engineering for the Design Reuse Group of Synopsys. The RMM Second Edition includes input from readers of the first edition who have gained experience in design reuse best practices, input from customers and independent reviewers. It also includes new guidelines on how and when it is best to use verification tools in the reuse process. The book also outlines strategies for verifying hard IP and for integration in a SoC. In addition, it contains an expanded section on model creation, physical integration and the design and implementation of reuse processes.

IP Core Reuse

SoC design, design reuse and verification promise unprecedented levels of productivity. Using pre-verified soft or hard IP cores for the design of multi-million gate SoCs involves the integration of proven elements. This contrasts dramatically to implementation and verification of what might otherwise be millions of separate gates and their connections. The term IP core refers to a design that can be viewed as a stand-alone sub-component of a complete SoC design. The term soft core refers to a soft macro or one that is delivered as synthesizable RTL code. When the term hard core is used, it refers to a hard macro or one that is delivered as a GDSII file. It is considered a hard core if it is already fully designed, placed, and routed.

Reuse is Now Required for Large De-signs and Short Product Life Cycles

Without IP reuse, the electronics industry will not be able to keep pace with the challenge of delivering the "better, faster, cheaper" devices consumers expect. The reusability of IP cores is a critical factor in the speed and predictability of IP integration, and significantly effects the success of an entire SoC project. IP reuse makes developing million-gate ASICs faster and with more predictable results. Purchasing soft cores and/or industry standard cores, such as IEEE 1394 - PCI32, from independent IP companies is often the best solution for creating these SoC designs, but evaluating IP is a new art required for SoC designs. RMM made the first attempt to guide the creation and evaluation of reusable IP cores. OpenMORE has the potential to change IP commerce because it makes IP reuse evaluation much easier.

Setting Guidelines

A key aspect of building a common IP infrastructure is devising a method to evaluate IP that can be widely-used. IP providers have designed their own rules and guidelines for IP reuse on a company-by-company basis. Today, many companies that buy IP to build libraries for reuse have also established evaluation procedures. Yet, these company-specific guidelines don't go far enough. A common reference system is needed to facilitate the engineer-to-engineer dia-log between companies - buyers and sellers of IP.

The Synopsys MORE rating system, based on the RMM, a Web-based tool, that measures a core's adoption of the RMM rules and guidelines, was a first step in this direction. The MORE assessment program, like the RMM, is a superset of company-specific rules and guidelines. MORE was developed to help IP companies improve their design processes and distinguish their designs from first-generation commercial IP, which was often difficult, risky and time-consuming to use. IP purchasers also can use the Synopsys IP Catalyst Catalog to view MORE ratings of commercial IP, including IP offered by the Mentor Graphics Inventra IP Divi-sion to identify IP that has been de-signed specifically for reuse. Some IP providers make the complete MORE assessment worksheets available to pro-spective customers to provide a com-mon understanding of the core.

OpenMORE Enhancements

OpenMORE adds new measurability criteria for design and verification of soft cores, extends to hard cores, and incorporates key hard deliverables specifications from the VSIA industry group. OpenMORE provides the industry's premier methodology to simply and quickly evaluate the reusability of IP cores for SoC design.
OpenMORE structures the assessment of the reuse quality of IP cores. IP developers enter assessment data into the worksheet following approximately150 rules and guidelines for soft cores and nearly 90 rules and guidelines for hard cores. Rules are assigned 5 points and guidelines are assigned 1 point. There are three categories used for the grading process: Macro Design Guidelines, Verification Guidelines, and Deliverable Guidelines. Designers are given the choice of answering each rule and guideline with A (always), N (never) or NA (not-applicable). A "not-applicable" response is allowed only for conditional rules and guidelines. The designer is given a total score out of maximum 730 possible points for soft cores and 530 points for hard cores. The result is an automatically assigned weighting and percentage for a final score. With this IP core assessment, IP providers are updating their design processes to adopt OpenMORE rules and guidelines and score higher results for their new IP cores, thereby raising the IP reusability level throughout the industry.

Working Closely with Industry

Mentor and Synopsys are working with industry groups to help establish a common reference for reusability in the industry. In addition to deliverables from VSIA Deliverables Document Version 2.0, work is underway with the Virtual Components Exchange (VCX), Design and Reuse, and VSIA who each have working or study groups addressing the broad area of IP quality. Mentor and Synopsys determined that it is beneficial for its SoC customers to collaborate to solve broad SoC industry barriers while maintaining closely aligned with these important industry groups. The benefits of this approach are leadership and responsiveness. Together Mentor and Synopsys can offer collaborative resources to address the needs of the fast-paced SoC industry, and at the same time, ensure that their measures are supported by the collective standards-setting processes of industry groups.

More information:
http://www.openmore.com/

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VSI Alliance Created Two New Working Groups

The VSIA Board has approved the formation of the Hardware dependent Software (HdS) Development Working Group (DWG) and a Platform-Based Design (PBD) Study Group to answer the needs of industry for embedded software reuse and emerging concept of platform-based design.
The HdS DWG will create specifications and standards for the reuse of software that depends on or controls the hardware in a chip, starting with taxonomy of embedded system design terminology.
The PBD Study Group will focus on creating a white paper on platforms, including an industry acceptable definition of SoC Platforms.
Participating in these groups is an important opportunity for many VSIA members.
To participate in the HdS DWG contact:
Co-Chairmen, Frank Pospiech (Alcatel) and Mikael Kaskowitz (Mentor Graphics) at hdsdwgchair@vsi.org.
To participate in the PBD Study Group, contact:
Co-Chairmen, Bob Altizer, (Motorola) and John Goodenough (ARM) at pbd-studygroup@vsi.org.

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New Smile at ECSI

Gabriela Bilincova is our new assistant at the ECSI Office in Grenoble, taking over duties of Judith Grassi and part of the duties of Florence Pourchelle. Gabriela is from Czech Republic and since last year she has been studying law, economy and languages at the Grenoble University. After she was graduated from high school in Prague, she spent a year at the University of Lausanne, Switzerland, and a year at the Connecticut College in Connecticut, USA, in order to improve her French and English. Before coming to France to retake her studies, she worked for an International Group in Prague as assistant of direction, where she obtained working experiences especially in the domains of international law and economy.
Besides her studies and a work at ECSI, she devotes her free time to sport as snowboarding, alpinism and hiking.

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The Unified Modeling Language

(Part 2)

by Alan Moore,
Artisan Software

Technical Solution – Design the System

In addition to the system definition constructed by analysing the requirements, it is necessary to construct a design for the solution, which describes the details of how the solution will be implemented. System definition and solution design may well overlap, which is acceptable as long as there is feedback and iteration between the two. The tworesulting models address the "what" and the "how" aspects of the required system.

Typically a high-level architectural design will be produced that forms the basis for a controlled, iterative, elaboration approach to developing the lower-level details. Several UML diagrams can be exploited during this stage. I will focus on the three primary design views of the system. They are Class Diagrams, Collaboration Diagrams, and State Diagrams.

Class Diagrams

Class Diagrams form the basis for the object architecture of the system, where objects identified in earlier analysis steps are organized into a set of interrelated classes with interfaces. The class icons on a Class Diagram have three possible parts: the class name, a list of attributes managed by the class, and a list of operations defined for that class. Classes can be packaged into larger groupings; the Plant Control package for example collects together all the classes involved in the core application domain. The static relationships between the classes are generalization, aggregation, and association. The generalization relationship captures the levels of abstraction of the object architecture.

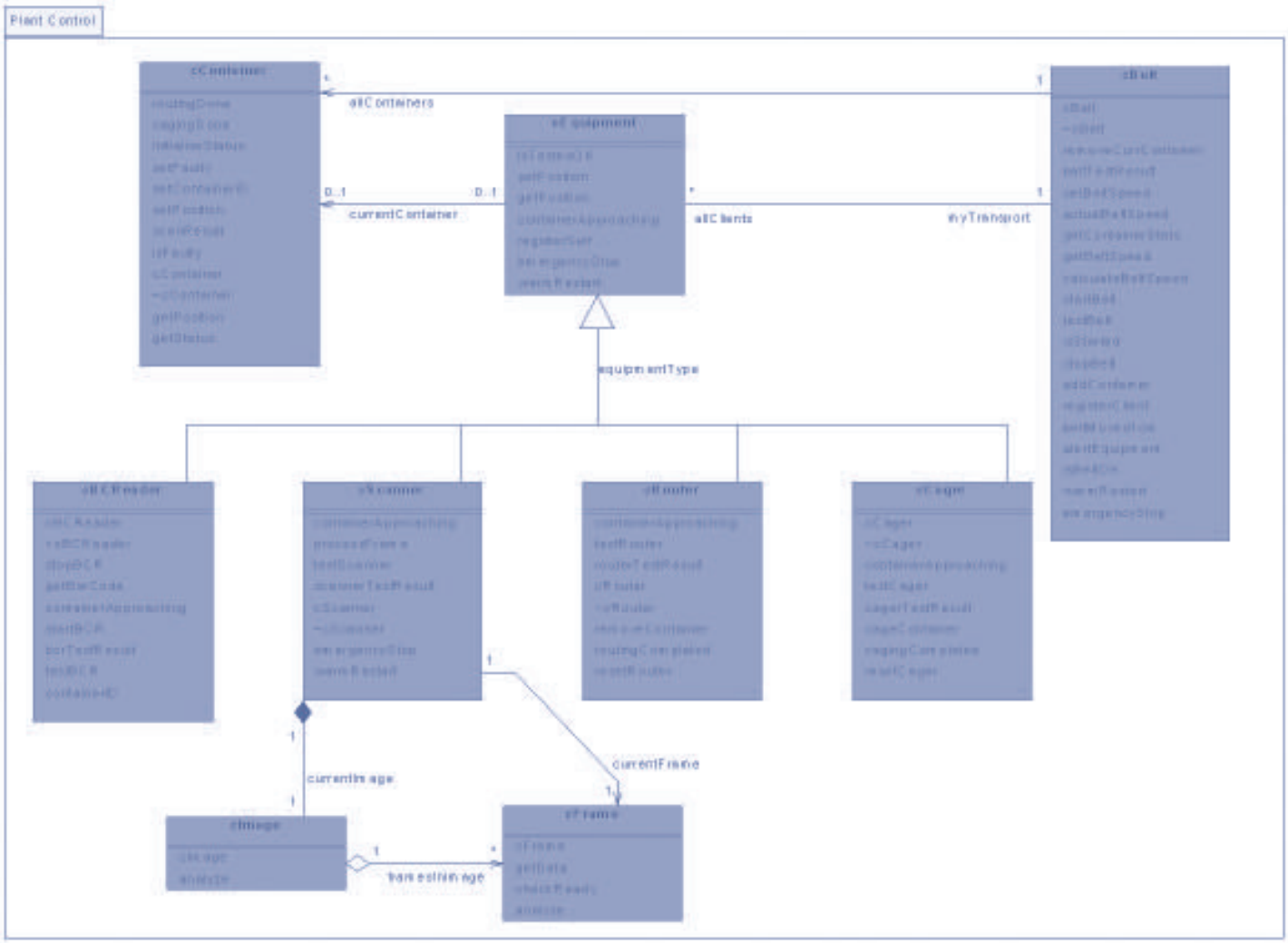

Figure 1 – Class Diagram

Through a hierarchy of super-class and sub-class relationships, the differences between object characteristics can be defined. The simple premise that a sub-class inherits all of the characteristics of its parent class allows for a powerful ability to "program by difference". This approach generalizes the common attributes and operations up the hierarchy and specializes the differences down the hierarchy. As shown in Figure 1, the cEquipment class hierarchy allows us to define a general-purpose piece of equipment that has standard operations. Each specific type of equipment in our system is built from the cEquipment parent.

The aggregation relationship provides the basic mechanism for composition. The fact that an object can be made up of other objects allows for convenient structural composition with clearly defined boundaries. By aggregating smaller, more specific objects into larger, more complex objects, overall system complexity can be managed using basic object-oriented principles. Figure 1 shows an example of an aggregation relationship in the construction the cImage class from its constituent cFrames.

Not all objects are part of a generalization hierarchy or aggregation, but in order for any two objects to interact (i.e., send messages) there needs to be some form of relationship between them. The association relationship provides the required mechanism for this. Figure 1 shows an example of an association between a piece of Equipment and the Container that it is currently processing. Clearly, there will be some communication between these objects and this relationship establishes the structure and visibility necessary to perform the messaging.

There are many characteristics of each of these relationships that further define their nature. Details such as multiplicity, visibility, role naming, and complex associative classes are beyond the scope of this article (see [1] for a good introduction).

Collaboration Diagrams

Where the Class Diagram defines a static relationship structure between the classes (and objects of those classes), the Collaboration Diagram defines a communication structure between the objects. Collaboration Diagrams can detail specific scenarios outlined in the Sequence Diagrams (above). The example shown in Figure 2 shows a specific scenario of scanning a container, where the numbers imply sequence.

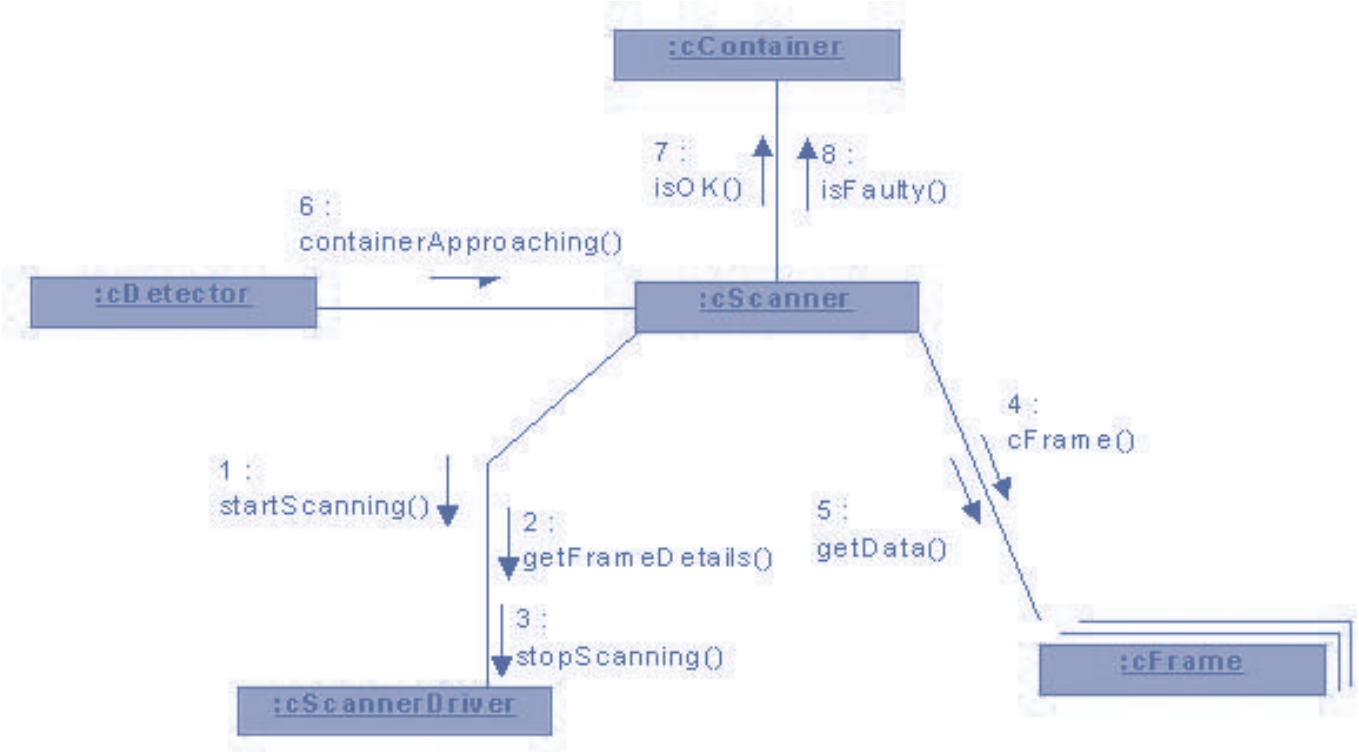

Figure 2 - Collaboration Diagram

By analyzing several Sequence Diagrams together as a whole and representing the overall connectivity of the objects involved in those scenarios on a Collaboration Diagram, it is possible to visualize the communication architecture of the proposed design. This view also facilitates the proper class relationship structures in the Class Diagram covered above since one could ask "… if these two objects are talking to each other, then what kind of relationship exists between them? …".

State Diagrams.

The state diagram is the principle diagram used in UML to describe the

behaviour of the objects in the class structure; these will be familiar to many electrical engineers although the UML uses a powerful form of structured state-chart based on the work of Harel[2].

In Figure 3 the various states of the cContainer object are shown; as it progresses along the belt each piece of equipment triggers a state change by sending an event, for example the scanner sends a scanResult that dictates whether the container needs to be specially routed or caged normally.

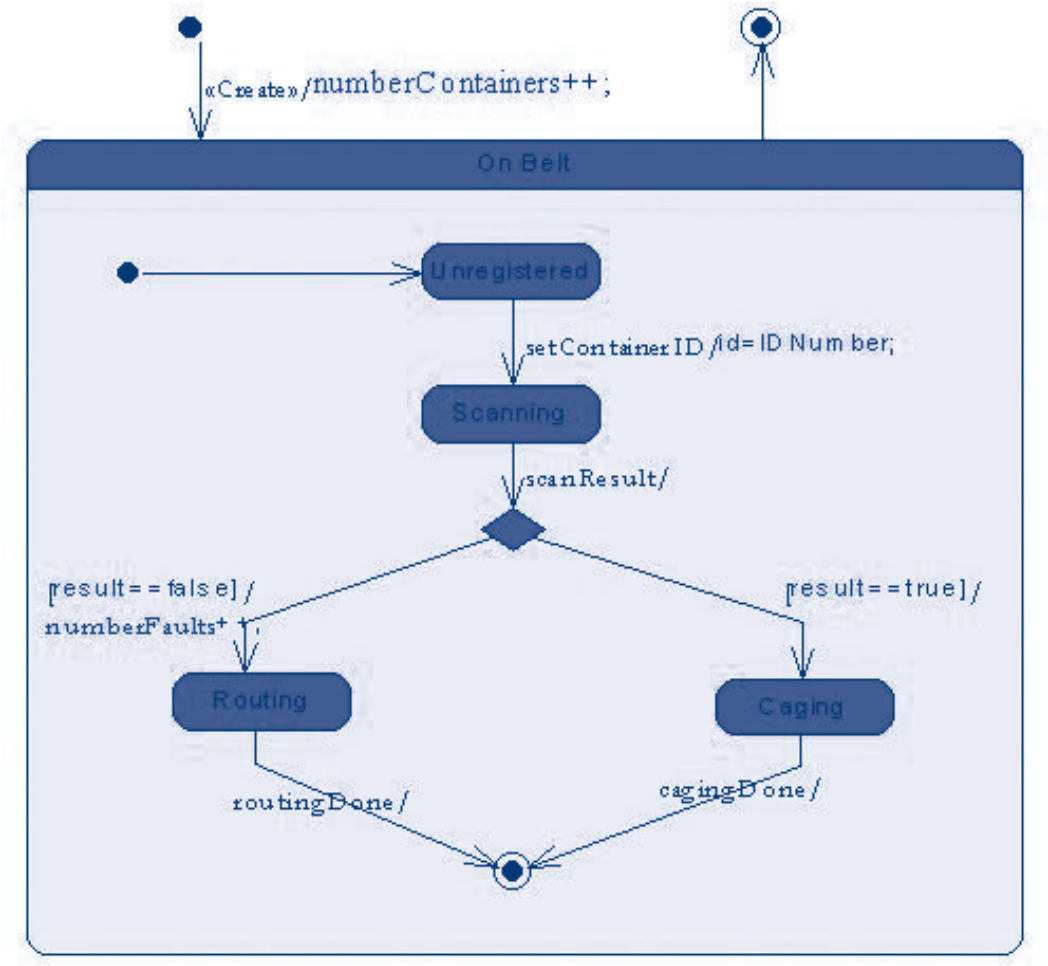

Figure 3 - State Diagram

UML also has the Activity Diagram, which uses a more flow-chart based approach to describing behaviour; in practice most control-oriented behaviour is better described by state diagrams.

Implementation

Two UML diagrams are used to show implementation, the Component Diagram, which is used to describe physical software artifacts such as executable programs and libraries, and the Deployment Diagram, which is used to document the actual hardware used. These diagrams are the simplest and least well developed of the UML diagrams; and urgently need improving to be useful to the real-time/embedded domain.

References

[1] Fowler, M. and K. Scott. UML Distilled. 2d ed. Reading, Mass.: Addison-Wesley, 1999.

[2] Harel, David. “Statecharts: A Visual Formalism for Complex Systems”, Science of Computer Programming, 1987; 8:231-274

News … News … News

Verilog Standardization

NAPA, Calif. — Implementation of the new Verilog-2001 hardware descrip-tion language became practical with the IEEE's release Wednesday (Oct. 17) of documentation that describes the standard, officially known as IEEE 1364-2001. Meanwhile, some EDA vendors are quietly moving ahead and adding support for Verilog-2001 constructs.

Although the IEEE approved Verilog-2001 in March, until now only a handful of people have had access to working versions of the documentation, said Dennis Brophy, chairman of the Accellera standards organization. "Now we have the authenticated version from the IEEE that's ready for the rest of the industry to use," he said.

Compared to previous versions of the language, Verilog-2001 promises to let designers work at a higher level of abstraction, and to achieve more timing accuracy for deep-submicron ICs. It also promises better simulation control and improved tool interoperability through an enhanced programming language interface (PLI).

While chip designers have yet to get up to speed on Verilog-2001, a few EDA vendors who have been involved in the standard's development are already moving ahead. For example, Cadence Design Systems Inc. has added some Verilog-2001 constructs to its PKS synthesis and NC-Sim simulation tools and will add more based on user demand, a spokesman said.

Co-Design Automation Inc. worked in parallel with the Verilog-2001 effort, and its Systemsim simulator supports Verilog-2001, said Simon Davidmann, chief executive officer of Co-Design. Superlog's additional language capabilities are "built on the Verilog-2001 base," he said. Mentor Graphics Corp. has implemented "substantial parts" of Verilog-2001 into ModelSim, said Anne Sanquini, vice president of Mentor's HDL design division.

Higher models, faster code

Behavioral extensions in Verilog-2001, Brophy said, are aimed at letting users create higher-level models and write code faster. He said that the addition of "configuration" blocks will allow for better design management and that "generate" statements, a concept borrowed from VHDL, will help prevent repetitious coding. Other new language features include multi-dimensional arrays, improved file I/O and re-entrant tasks.

To support more accurate ASIC and FPGA timing, Verilog-2001 adds support for on-detect pulse error propagation, negative pulse detection, new timing constraint checks, negative timing constraints and enhanced Standard Delay Format (SDF) support. The Verilog Charge Dump (VCD) file format has been extended beyond four states to support more detail on net strength and port changes.

New features added to the Verilog programming interface (VPI), which is part of the PLI, provide improved control over simulation and debugging, Brophy said. He also noted that new VPI functions allow for better integration of C language models.

The PDF version of the IEEE standard 1364-2001 is available now, with the print version coming in late October. These can be ordered at www.ieee.org.

1364.1 Verilog Synthesis In-teroperability Working Group: Status DAC'01

• WG has been reactivated following approval of 1364-2001 standard
• Newly added features being considered for synthesis
• Teleconference meetings set for every month starting July'01
• Goal is to have a final draft ready 2Q2002
• Our web site:
http://www.eda.org/vlog-synth
• Any questions? Send to Chair:
J. Bhasker <jbhasker@cadence.com>

SystemC 2.0 Available

The version 2.0 of SystemC standard is now available for download at:
http://www.systemc.org/

GLOSSARY

ASIC
Application Specific Integrated Circuit

DWG
Development Working Group

ECSI-SYDIC
ECSI SYstem Design Industry Council

EDA
Electronic Design Automation

HDL
Hardware Description Language

IFIP
International Federation for Information Processing

IP
Intellectual Property

OMG
Object Modeling Group

PLI
Programming Language Interface

RMM
Reuse Methodology Manual

SDF
Standard Delay Format

SLDL
System Level Design Language

SLI
System Level Integration

SLM
System Level Macros

SOC
System-On-Chip

SSDL
System Specification and Design Languages

SYDIC-Telecom
SYstem Design Industry Council for Telecom Industry

UML
Unified Modeling Language

VC
Virtual Component

VSIA
Virtual Socket Interface Alliance

WG
Working Group

CALENDAR OF EVENTS

DECEMBER 2001

3-5

IFIP VLSI-SOC 2001
11th IFIP International Conference on Very Large Scale Integration
The Global System on Chip Design & CAD Conference
Montpellier, France
http://www.lirmm.fr/vlsisoc01

6-8

International Workshop on IP Based Synthesis and SoC Design
Grenoble, France

JANUARY 2002

7-11

VLSI 2002 & ASP-DAC 2002
15th International Conference on VLSI Design and 7th Asia and South Pacific Design Automation Conference, Bangalore, India
http://vlsi.ccrl.nj.nec.com

23-25

Z/B2002
2nd International Conference on B and Z Users
Grenoble, France
www-lsr.imag.fr/zb2002

MARCH 2002

4-8

DATE 2002
Design, Automation and Test in Europe Conference & Exhibition
Le Palais des Congres, Paris
www.date-conference.com
Meetings:
- ECSI-SYDIC Meeting
- 5th European SystemC Users Group Meeting
  www-ti.informatik.uniuebingen.de/~systemc/

4

TECHNODAT
MEDEA+ Project T-101 Technology-driven Design and Test Workshop, Paris, France
Philippe.Garcin@st.com

8

MESA
MEDEA+ Project A-502 Multi-processor Embedded Systems Architectures, Paris, France
Philippe.Garcin@st.com

18-20

ISQED'2002
3rd IEEE International Symposium on Quality Electronic Design
San Jose, California, USA
www.isqed.org

APRIL 2002

17-19

ICCDCS 2002
Fourth IEEE International Caracas Conference on Devices, Circuits and Systems
Seaport Conference Center, Aruba, Dutch Caribbean
http://pancho.labc.usb.ve/iccdcs2002

25-26

ISVLSI 2002
IEEE Computer Society Annual Symposium on VLSI
Pittsburgh, USA
www.cs.uga.edu/~bishop/isvlsi/

27-29

ACL2-2002
Third International Workshop on the ACL2 Theorem Prover and Its Application
www.cs.utexas.edu/users/moore/acl2/workshop-2002/

MAY 2002

23-24

EWME 2002
4th European Workshop on Microelectronics Education
Parador de Baiona, Mancomunidad de Vigo, Spain
www.ewme2002.org

JUNE 2002

10-14

DAC2002
39th Design Automation Conference, New Orleans, USA
www.dac.com

JULY 2002

6-7

SOCRT 2002
Workshop on System-on-Chip for Real-Time Applications
Banff Conference Center, Banff, Canada
www.socrt.org

1-3

RSP2002
13th IEEE International Workshop on Rapid System Prototyping
Darmstadt, Germany
www.rsp-workshop.org

AUGUST 2002

25-30

WCC 2002
IFIP Congress 2002 - 17th World Computer Congress
Montreal, CA
contact-wcc2002@cips.ca
http://www.wcc2002.org

SEPTEMBER 2002

4-6

DSD'2002/Euromicro
Symposium on Digital System Design: Architecture, Methods, and Tools
Dortmund, Germany
http://www.co.umist.ac.uk/dsd2002

24-27

FDL 2002
Forum on Design Languages
IMT, Marseille, France
www.ecsi.org

24-26

ESSCIRC 2002
28th European Solid-State Circuits Conference
Florence, Italy
http://ele.unipv.it/esscirc2002

OCTOBER 2002

27-29

HLDVT'02
High Level Design Validation and Test Workshop
www.cse.ucsd.edu/groups/hldvt/02/

JANUARY 2003

VLSI 2003
16th International Conference on VLSI Design
New Delhi, India
http://www.vlsidesign.org or
http://vlsi.ccrl.nj.nec.com.

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