



Is SoC design always costly and complex, with quality problems? Not always. By **Louise Joselyn**.

It is often said that designing SoCs with IP blocks from third party vendors is fraught with problems. The design process is horrendously complex, particularly when it comes to verification, they say. Appropriate design tools are either not available, hideously expensive or do not work as intended. The acquisition of IP is time consuming, requires advanced legal skills, IP quality is variable, particularly from smaller vendors, and technical support is a lottery.

Of course, all this can be true, but not necessarily across the board. To provide a balance, it is useful to recognise that IP based SoC design is becoming a more viable approach for a wide range of designs, not just for the smallest, fastest, most complex circuits fabricated on the most advanced processes.

Take the 8051 cpu, for example. There are at least 45 variants of the 8051 from some 20 vendors listed on the Design & Reuse IP portal. Interest levels are high

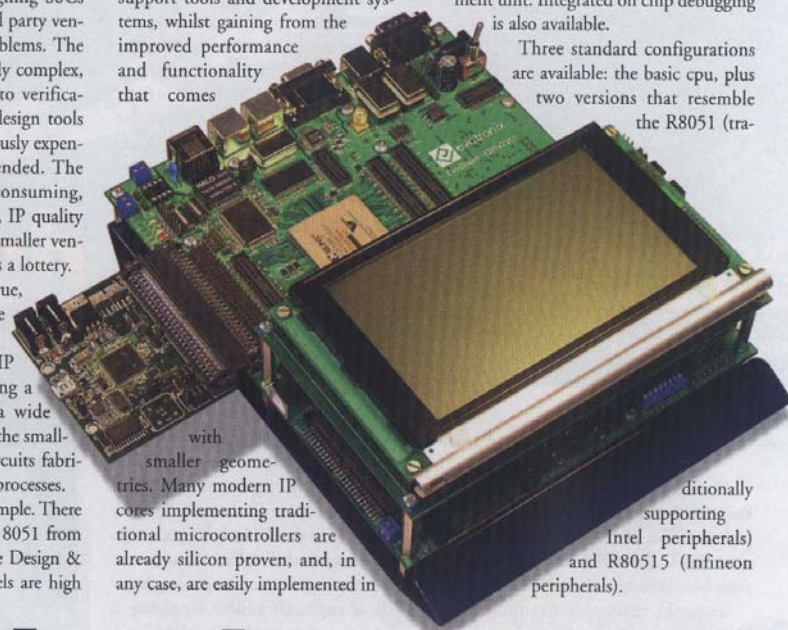
as an effective solution to replacing obsolete and obsolescent discrete devices.

Many engineers are now tempted to take advantage of their years of experience in designing with traditional device architectures – the devil they know. They can exploit a wealth of legacy software, support tools and development systems, whilst gaining from the improved performance and functionality that comes

with smaller geometries. Many modern IP cores implementing traditional microcontrollers are already silicon proven, and, in any case, are easily implemented in

original 80C51 as instructions are completed in fewer clock cycles. Configurable options include: software and hardware interrupts; serial, i²c and spi interfaces; watchdog timer; additional 8bit I/O ports; a multiplication and division unit; and a power management unit. Integrated on chip debugging is also available.

Three standard configurations are available: the basic cpu, plus two versions that resemble the R8051 (tra-



ditionally supporting Intel peripherals) and R80515 (Infineon peripherals).

The devil you know

and increasing – not only for the 8051, but also for other traditional cores, such as PIC, Z80 and 80186 architectures.

Partly, this is because the IP based SoC design methodology is better established and understood, but also because more affordable tools are available, not only from eda vendors, but also from IP providers, fpga vendors and even foundries. Meanwhile, the reputation of many IP vendors is improving. In addition, the IP route is fast being recognised

fpgas for evaluation, verification and development purposes, and for low to medium volume production.

Many offer superior performance and flexibility, yet retain full backward compatibility. Take the latest announcement from Polish company Evatronix. The R8051 is a configurable core which can be tailored to meet specific requirements, executing the popular MCS51 instruction set. However, it offers, on average, eight times the performance of the orig-

“We’ve seen demand for our ‘risc like’ versions of 8051 cores increase over the last couple of years,” said Wojtek Sakowski, Evatronix’ president. “In fact, most previous customisation has been to remove peripherals, which is why we developed a configurable peripheral set.”

Above: Evatronix’ demonstration and validation boards are proving useful for customers as development platforms.



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Wojtek Sakowski, **Evatronix**

Recently, Evatronix has expanded its range of IP cores, and recent introductions include a USB On the Go block, certified according to USB-IF procedures, an Ethernet MAC block and other serial links.

Sakowski maintains Evatronix' IP blocks compare favourably with any on the market. When it comes to service and support, he believes Evatronix can often do better.

The company has implemented a design flow aimed at producing quality designs, underpinned by ISO9001 procedures. "We have adopted the Reuse Methodology Manual rules formulated and recommended by Synopsys and Mentor Graphics," Sakowski explained. "Peer review techniques are applied to design specification and source code modules to capture most errors before simulation starts." HDL models are tested against reference chips (where appropriate) by means of a hardware modeller. TransEDA tools are used to perform static rule checks and code coverage for test suites. In fact, Sakowski

insists documented verification plans and test plans govern the verification process.

The company has begun to adopt VSIA QIP rules, which provide an independent measure of IP quality and an assessment of IP provider development and quality procedures. For standards based IP, such as USB blocks, Evatronix designs are subjected to an external certification process.

Evatronix' cores are prototyped in fpgas and reference designs are developed for demonstration and final validation purposes. The boards, containing cpu cores – including ARM in Altera Excalibur, USB, peripherals, display controllers, interfaces and interconnect circuitry – are proving useful as development platforms. The company also offers evaluation boards for 8/16bit and 16/32bit environments. "It's not enough to supply top quality IP cores on their own, customers are demanding high levels of support. And many are fed up with the lack of service from larger vendors," Sakowski commented.

Regarding technical support and service, there is an argument that SoC designers are more likely to be able to talk directly to the IP block designer with a smaller company like Evatronix, than it can with a large vendor, employing hundreds of engineers and/or supplying a wide range of cores that it might have acquired, rather than developed in house. Evatronix has a partnership arrangement with Europractice for prototyping and low volume multiwafer production runs for academic and commercial clients, called IP@prototype.

Smaller IP vendors like Evatronix can often be more flexible in terms of licensing and royalty schemes. For fpga implementation, for example, Evatronix offers its FpgaEasy4U programme, providing simpler licensing, and lower pricing for Xilinx and Altera solutions. "Most of our business to date has been in ASIC implementation, but we have some good potential customers for fpga. Unfortunately, most are simply not fully aware of the benefits of IP for fpga, but it will come," Sakowski said. Larger, long standing IP vendors, such

as ARM and Rambus, have always been aware of the high levels of support needed. In fact, both have recently made moves in the eda arena. The implication is that currently available tool suites may not meet all the demands of their major customers.

ARM, not surprisingly, can call upon an entire ecosystem of support tools and services, not only from its in house portfolio, but also from a large and growing number of third party partners. Whilst ARM works closely with eda tool vendors, such as Synopsys, it is also delving into that activity itself with its acquisition last year of Axis and its RealView esi (electronic system level) design tool. ARM also contributes significantly to international standards efforts, being a founder member



of Spirit and a key player in the latest ECSI initiative, Sprint, to develop transaction level modelling (TLM) standards and methodology to integration, verification and debugging of SoCs at the electronics systems level.

Meanwhile, Evatronix is keeping pace with technology and methodology changes, such as the adoption of techniques such as TLM. "Quality and efficiency are strategic efforts and contribute toward our evolving competitive advantage," Sakowski concluded. ☺