

PRODUCT CATALOG

8051 ISA-compliant Platform

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Hot!

R8051XC2

World's fastest 8051 microcontroller

- ◆ Over 12 times faster than Intel™ 80C51
- ◆ Fully configurable
- ◆ Straightforward application debugging with EASE
- ◆ Available now

8-bit Configurable Platform for System-on-Chip designs based on 8051 Instruction Set Architecture


 **R8051XC2** — the world's fastest, user configurable 8-bit microcontroller that is instruction set compatible to Intel™ 8051 microcontrollers. The controller achieves up to 12.1 times higher performance rates than the original chip when working at the same clock frequency. The peripheral set is fully configurable and easily adjustable. Intel 8051 and Siemens 80C515/80C517 compatible blocks are included, and so are the following powerful peripherals — I2C, SPI, DMA and RTC. For better value with no sacrifice of performance fixed versions of R8051XC2 are also available.


Configurability


Configuration spreadsheet provided with every configurable version of the IP core enables the user to define all configuration details, e.g. what peripherals to use, what interrupt controller architecture should be applied, how many data pointers should be provided and so on. As a result, an estimated gate count for the custom configuration version is given. The multiuse license for the configurable version gives the customer access to the Design Configurator for self-conducted use.

Features & options




- ◆ Program and Data Memory size extension
- ◆ Up to 8 Data Pointers with arithmetic support
- ◆ Software Reset
- ◆ Possibility to exclude a few rarely used instructions
- ◆ Flexible DMA controller
- ◆ SPI and I²C™ serial ports (with software drivers)
- ◆ Real Time Clock circuitry

 **R8051XC2-A** — downwards configurable version of the R8051XC2 IP core with the Intel™ 80C51 chip compliant peripheral set. Also available in a fixed configuration.


 **R8051XC2-B** — Siemens™ 80C515 and 80C517 compatible and downwards configurable configuration of the R8051XC2. Also available in a fixed configuration.

 **T8051** — derived from the successful R8051XC architecture, the T8051 is the world's smallest 8051 ISA-compliant IP core. Its CPU with less than 3.000 gates can easily serve as a replacement for hard-coded control FSM.

Software development support

-  **Third-party tool support:** All the features are fully supported by Keil μVision 3.
-  **Debugging:** The R8051XC2 can be enhanced with the Evatronix Application-debugging Support Environment (EASE) . The EASE consists of a built-in On-Chip-Debug-Support (OCDS) module, USB Debug Pod for communication with host computer and Evatronix Debug Interface software plug-in for interfacing the instrumented microcontroller to Keil μVision IDE.
-  **RTOS support:** The Micrium μC/OS-II RTOS has been successfully ported to the R8051XC2 platform.

Development environment

 **R8051XC2-Demo-A** — a real application based evaluation system demonstrating the R8051XC2 functionality.

Solutions with previous generation R8051XC

R8051XC-A — fully functional 8-bit embedded microcontroller that executes all ASM51 instructions and is compliant with the 80C51. The R8051XC-A version provides interrupts, an interface for serial communications and two timers.

R8051XC-B — the R8051XC-A microcontroller with Timer2 with CCU, more interrupts, Serial 1, Watchdog and a 4-level interrupt priority decoder; compliant with 80C515/517.






USB Full Speed Connectivity — an integrated solution containing Evatronix R8051XC IP core with USB Full Speed device controller and an optimized software stack which speeds-up development of the USB Low/Full-Speed applications.

USB High Speed Connectivity — a similar product tuned for the USB Full/High-Speed applications.



Embedded Ethernet — a design made for quick deployment of embedded Ethernet applications. It integrates R8051XC, the Ethernet MAC IP core and a third party TCP/IP stack.

HDLC Connectivity — R8051XC and HDLC controller combo IP ready to use base for development of a complete HDLC protocol and derivatives-based solutions.

USB device & OTG Controllers

-  **CUSB** — USB Full-/Low-Speed function controller compatible with USB 2.0 Specification and supporting serial interface for USB PHY and generic read/write parallel interface for CPU. Available also with AMBA™ AHB interface and optional DMA.
-  **CUSB2** — Fully configurable USB 2.0 Hi-Speed function controller supporting UTMI and ULPI interfaces for USB PHY. In addition to the CPU interface it provides FIFO port which is used to speed up USB data transfers.
-  **USBHS-OTG-SD** — USB 2.0 On-The-Go Dual Role Device controller, which adds On-The-Go Host functionality to the CUSB2 controller and supports all operating speed rates.
-  **USBHS-OTG-MPD** — USB 2.0 On-The-Go Dual Role Device controller with Hub support. It also contains USB protocol-aware DMA engine and FIFO latency buffers to improve performance and decrease number of logic gates.
-  **USBHS-HUB** — a feature-rich, configurable USB 2.0 hub controller that provides an interface between a USB host and multiple USB devices, each of which can operate with different signaling frequencies - Low-, Full- or Hi-Speed.

USB Software Stack and class drivers

-  **Generic USB Software Stack** written in ANSI-C Software Stack and independent from the CPU, operating system and USB controller.
-  **Optimized versions of the USB Software Stack:**
 - ▶ Optimized for CUSB and 8051 microcontroller
 - ▶ Optimized for CUSB2 and 8051 microcontroller
 - ▶ Optimized for USBHS-OTG-SD and 8051 microcontroller.

Each package contains example drivers for most popular USB classes.

Development environment

Development environments provided by Evatronix consist of the particular USB controller, USB Software Stack that runs on one of Evatronix processor cores, example application and Evatronix evaluation board. The available software allows rapid creation of designs for such USB classes as Mass Storage, HID and Audio/Video.

PHY/transceiver interoperability program

Evatronix USB controllers were used with a number of third party PHYs and transceiver ICs. Evatronix performs USB-IF compliance pre-testing to discover and solve any issues regarding interoperability between its controllers and third party USB PHYs.

USB customization services

Under service contracts Evatronix provides customization of existing Evatronix USB controllers and development of user application firmware.

Certification support service

To confirm full compliance of our Evatronix USB controller cores to the USB specification we submitted successfully many reference designs containing our cores to the USB Implementors Forum certification procedures. Experience gained in this process allows us to assist our licensees in winning the USB compliance certificate.









USB Connectivity platforms

Full Speed Connectivity — pre-integrated solution based on USB FS/LS function controller, R8051XC microcontroller and optimized software stack.

High Speed Connectivity — similar solution for USB high speed applications.

C68000AHB-OTG-MPD — pre-integrated solution which contains the C68000 microcontroller and the USB On-The-Go Dual Role Device controller.


Ethernet Media Access Controllers

-  **MAC-1G** — the most feature-rich controller in the family. Operates at 10/100/1000 Mbps speed modes, and contains the integrated descriptor based DMA. Its features include: MII PHY management, Flow Control, and a full set of Statistical Counters.
-  **MAC-1G-Lite** — the controller optimized for small size. It shares the speed of MAC-1G but has reduced complexity. It communicates with the host using the direct FIFO interface.
-  **MAC** — the basic controller in the family. It operates at 10/100 Mbps speed and contains the integrated descriptor based DMA.
-  **MAC-Lite** — the smallest product in the family. Shares the speed modes of MAC 10/100 but with reduced complexity. It also communicates with the host using the direct FIFO interface.
-  **MAC-1G-PCS** — The MAC-1G PCS is an IP core of a 1 Gigabit Physical Coding Sublayer (PCS) that meets all IEEE 802.3-2002 Standard requirements. The MAC-1G PCS provides both PCS interfaces - GMII and PMA. It also features the Management Interface (MGM) for communication with the Station Management (STA).
-  **P1588** — The IEEE 1588 protocol controller that provides a standard method to synchronize devices on a network with sub-microsecond precision — key in consumer applications or control and measurement systems.

Optional interfaces

Host processor interfaces for DMA based products	PHY interfaces
Generic	GMII
AMBA™ AHB/APB	MII
OPB	RMII
Wishbone	SMII
Avallon (SOPC ready)	

Software Drivers

 **MAC eCos Driver** — the reference software driver for the eCos RTOS; interfaces to eCos TCP/IP stack.

 **MAC & MAC-1G Linux Driver** - the software driver for Linux operating system.

Both drivers come with the complete ANSI-C source code and all documentation. Typically used on dedicated operating systems but drivers also work as an example when writing user application software.

Ethernet customization services








Every standard product can be customized according to specific user application requirements. The customization options include changing the network/host interfaces or extending functionality of the core. We can modify the behavior of our DMA engine or provide hardware acceleration of a higher level protocol, like for example TCP/IP.

SoC Development Platform




Embedded Ethernet Platform — a complete solution that integrates R8051XC-MAC-L-HA controller with the CMX-MicroNet™ TCP/IP stack. For off-loading the host microcontroller, generation and analysis of checksums are implemented in hardware. It minimizes the effort of adding an internet connectivity to an embedded product. The web server application demo shows the typical use - controlling embedded systems remotely via the internet.





Memory Controllers

-  **SDIO-HOST** — The SDIO-HOST is an SD/SDIO/MMC host controller compatible with the SDIO Host Specification version 2.00. It supports SD Memory Card 2.00, SDIO Card 2.00, and MultiMediaCard 4.2.
-  **SDIO-HOST Software Driver** — a complete software packet that supports SDIO Host Controller IP core that allows user to build applications without detailed knowledge of SDIO Host controller hardware.
-  **NANDFLASH-256** — a NAND Flash memory controller. It allows connection of up to eight Flash memories to the AMBA™ AHB interface. It facilitates use of the NAND Flash devices in various embedded systems.
-  **NANDFLASH-CTRL** — the state-of-the-art version of the NAND FLASH Controller which supports large SLC & MLC memories and features advanced 16-bit BCH error correction mechanism as well as full ONFi support. The controller is available with OCP interface and wrappers for other bus standards.
-  **NANDFLASH-CTRL Software Driver** — the NAND Flash controller driver designed to enable full functionality of the NAND Flash controller.
-  **ATAIF** — dedicated ATA Host Controller designed for embedded systems. It provides a simple interface to hard-disk drives, DVD & CDROM players/writers, CompactFlash and PC-Card devices. The ATAIF supports all PIO modes, Multi-word DMA modes and Ultra ATA (up to UDMA133).
-  **ATAIF Software Driver** — a complete software set dedicated for handling Evatronix ATA Host Controller.



Data Communication

-  **SDLC** — a controller handling the SDLC protocol which is a subset of HDLC protocol. It interfaces with the host using generic bus and several interrupt lines. The core is also available with AMBA™ APB interface.
-  **HDLC** — hardware implementation of two full-duplex HDLC channels. It integrates SDLC with the hardware support for LAPB/LAPD protocols (auto I and S frame handling). It interfaces with the microprocessor through a generic bus.
-  **HDLC Connectivity Platform** — designed to ease the building of an 8051-based HDLC microcontroller and to offer ready to use reference design as a base for development of a complete HDLC protocol and derivatives-based solutions.



FireWire® Link Layer Controller

-  **C1394A** — a link layer controller for IEEE 1394a serial bus (FireWire®). It handles asynchronous and isochronous traffic, supporting up to 4 isochronous channels. It has a dedicated interface for high-speed direct data transfer which reveals the processor from high bandwidth data transfers. It is AMBA™ APB interfaced.
-  **C1394A Software Stack** — the C1394A Software Stack implements transaction and bus management layers of IEEE 1394a serial bus. It is dedicated to work with the C1394A core - an IEEE 1394a link layer controller.





Audio transmission

-  **SPDIF** — audio transmission controller that meets the IEC™ 60958-1 International Standard. It may operate as receiver or transmitter, supporting transmission rates from 3kHz to 192kHz. Also integrated with AMBA™ APB or AHB bus.
-  **I2S** — the interface which supports a majority of the I2S transmission modes. There are eight stereo transmission channels in the core, which each have the ability to operate as a receiver or transmitter. The transmission rates range from 22.05kHz to 192kHz and it is integrated with AMBA™ APB as well as the AHB and OPB bus.

Display Controllers

-  **DISPLAY-CTRL** — a VGA display controller which enables resolutions up to WUXGA 1920x1200 pixels. It supports programmable resolutions and timings that are limited only by the SoC's bus bandwidth. Its analog VDAC interface is compatible with Analog Devices™ ADV7120. Lastly, the microprocessor and memory interfaces are integrated with AMBA™ AHB bus.
-  **TVOUT-CTRL** — a TV display controller that follows the ITU-R BT601/BT656 recommendation and is dedicated for using with Analog Devices™ ADV7174/79 encoder video chip in PAL and NTSC systems. The microprocessor and memory interfaces are integrated with AMBA™ AHB bus.

Serial Bus Interfaces

-  **I²C** — I²C™ bus controller which meets the Philips™ I²C bus interface specification. It may also operate as receiver or transmitter in a master or slave mode. It supports transmission rates of up to 400 kHz and the core is available with a generic as well as AMBA™ AHB interface.
-  **I²CS** — I²C™ bus controller which meets Philips™ I²C bus interface specification. It is a slave controller that may receive and transmit data with transmission rates up to 400 kHz.
-  **I²C-HS** — I²C™ bus controller which provides a serial interface that meets the Philips™ I²C bus specification v.2.1. This core can work with high-speed mode transmission (up to 3.4Mb/s) which provides backward compatibility with a standard mode (up to 100kb/s) and fast mode transmission (up to 400kb/ s). The core is available with generic as well as AMBA™ AHB interface.
-  **SPI-MS** — Serial Peripheral Interface which supports slave as well as master capability with its own baud rate generator. It has a programmable serial clock and a dedicated set of slave selection signals which facilitates integration in a multi slave system.



Obsolete parts replacement

Since its foundation in 1997, Evatronix Electronic Design Department has gained extensive experience in designing IP cores with pin-to-pin equivalency to the existing hardware chips.

The company has developed a set of procedures for integration of hardware modeling technology into the IP development process. These procedures assume the use of advanced software and hardware tools for precise modeling of behavioral and functional features of the original component. The hardware tools applied to the process enable engineers to analyze the original chip's behavior with clock-by-clock precision, visualize it and then transfer into the developed replacement. Integration with verification environments from various EDA vendors guarantees the highest level of IP core's compliance with the original chip. Our Personal Hardware Modeler is integrated with a third-party simulation software to ensure seamless operation of developed IP replacements.

All replacement cores below are available as off-the-shelf products with the relevant documentation. They may also be treated as a base for further development or modifications to suit customer's application.

Original device	IP core	Notes
Z80-family based Microprocessor & Peripherals		
Zilog™ Z80 CPU	CZ80CPU	8-bit microprocessor
8-bit Microprocessors		
MOS Technology™ 6502	C6502	8-bit microprocessor
16- & 32-bit Microprocessors		
Intel™ 80c186xl	C80186XL	16-bit microcontroller
Intel™ 80c186	C80186	16-bit microcontroller
Motorola™ MC68000	C68000 ¹	16-/32-bit processor
DSP & Numeric Coprocessors		
TI's TMS320C25™	C32025 ²	16-bit fixed-point DSP
Intel™ Intel387SX	C387L	numeric coprocessor dedicated for 80386

¹**C68000-AHB** - a version of the C68000 which implements AMBA® AHB interface protocol compatibility; thus 32-bit data and data address buses are available for external components.

C68000 On Chip Debug Support— the C68000 and C68000-AHB microprocessor cores are available with Evatronix On Chip Debug Support module for fast and efficient application debugging solution.

²**C32025TX** — a version of the C32025 core executing most of instructions in a single clock cycle.

IP on demand

With its extensive expertise in the area of IP core development, Evatronix is ready to design any IP product the customer is looking for. The engineers may follow the specification the customer provides us with or create new value from scratch, given only its final functionality requirements.

IP on demand service gives the customer total control over IP development. Product specification, project schedule and the list of requested deliverables are prepared in tight interaction with the customer in order to fully meet his needs and fit the amount and pace of work into his design flow.

FPGA design

Evatronix has been using FPGA-based prototyping for final verification of the IP cores since it entered the silicon IP business in 1997. Over these years Evatronix engineers have gained essential experience in development of Systems-on-Programmable-Chips (SoPCs) by creating IP evaluation solutions, demos or reference designs depending on customer's needs.

The design consists of the state-of-the-art FPGA chip embedded in the Evatronix proprietary hardware environment with an evaluation board, variety of adapters and the Evatronix Application-debugging Support Environment (EASE), thus being one of the most complete solutions on the market. It can be further enhanced by proprietary or third-party software - operating systems, peripheral drivers or software stacks.

Standard deliverables

- ◆ VHDL or Verilog RTL source files (soft core license only)
- ◆ Post-synthesis netlist targeted at FPGA technology of choice (firm cores license)
- ◆ Compiled simulation model (optional for netlist versions)
- ◆ A synthesizable top level design that instantiates technology with dependent components such as tri-state buffers and memories (if needed)
- ◆ Complete VHDL or Verilog testbench (contains examples of instantiation of the core and a set of test bench elements — stimulators, comparators, monitors, etc.)
- ◆ Test Suite, a set of test cases that run within the test environment. It covers all the core's functions which are listed in the Test Plan
- ◆ User documentation set
- ◆ A set of simulation support scripts and macros
- ◆ Synopsys Design Compiler support
- ◆ Place & Route scripts and constraint files for Altera & Xilinx FPGA families (optional for source code delivery)

Business models & support

Our products are licensed as:

- ◆ soft cores with full source code delivery
- ◆ firm cores with technology specific netlist delivery

Single project license — license for a single design without volume limitation. The reuse fee is charged for any further consecutive design.

Multiple project license — license for an unlimited number of designs without volume limitation.

Prototyping/limited volume license — license for a single design with limited volume of final devices/chips, dedicated mainly for FPGA design or ASIC prototyping.

Support — standard 30 days of service is covered by a license fee. Extended support can be purchased at extra cost.

Any specific business model can be discussed on demand.

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