

SDIO-HOST

SD/SDIO/MMC/eMMC Card Host Controller

Overview

The SDIO-HOST is an SD/SDIO/MMC/eMMC host controller compatible with the SD Host Specification version 2.00. It supports SD Memory Card 3.00, SDIO Card 2.00, and MMC/eMMC 4.4 specifications.

The configurable multi-slot architecture makes the design suitable for a wide range of applications, including very low area designs. The silicon space requires below 33k gates for the simple single-slot configuration without DMA, or 69k gates for the 4-slot version with Advanced DMA. Each slot can be individually controlled through the Standard Register Set.

Applications

- ◆ HD Video storage
- ◆ Handheld consumer electronics
 - Digital cameras
 - Camcorders
 - Digital audio players
 - GPS receivers
 - Cellular phones
 - PDAs
- ◆ Consumer electronics
 - USB SDIO dongles
 - Sensor applications
- ◆ SoC design interfacing with SDIO Cards or ICs, such as:
 - 802.11b modems
 - Digital TV tuners
 - Fingerprint recognition cards

Features

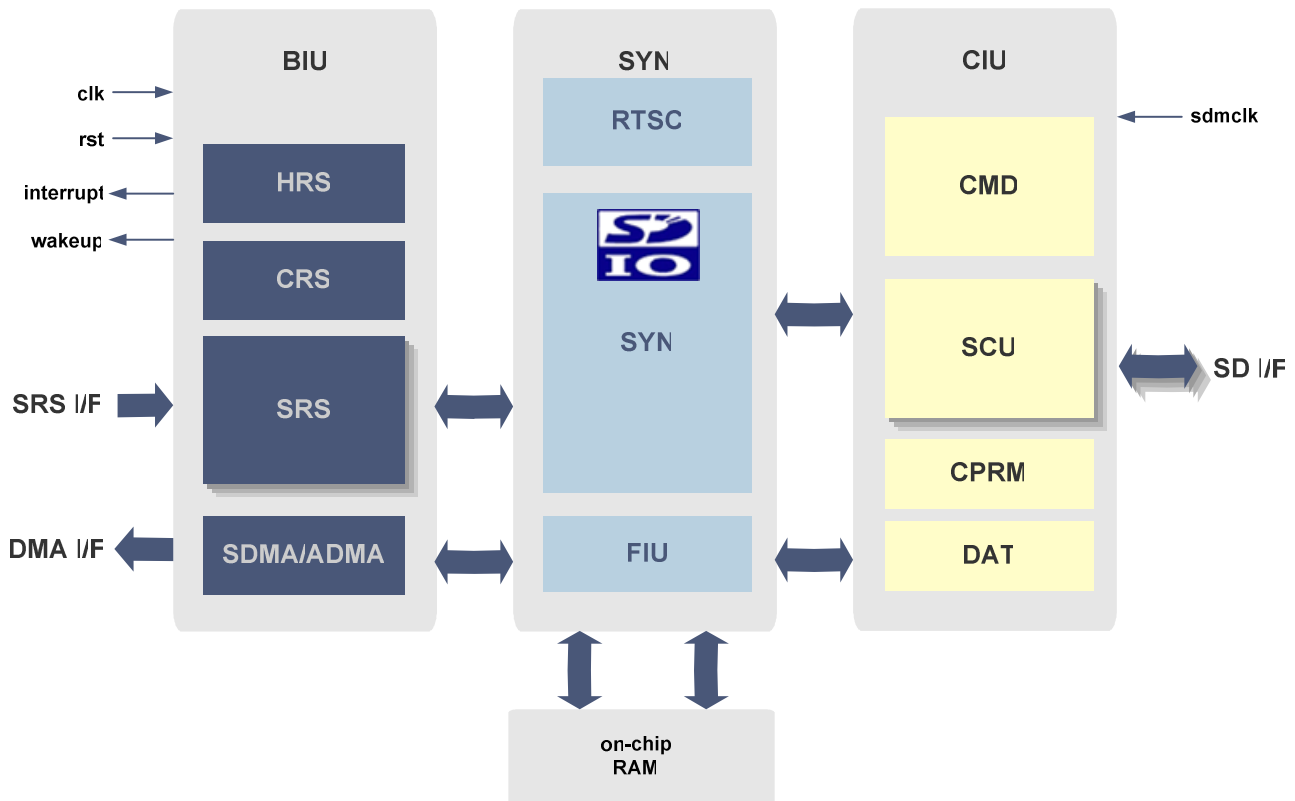
- ◆ Compatibility
 - SD Memory Card version 3.00 (SC, HC and XC cards)
 - SDIO Card version 2.00
 - MMC/eMMC Card version 4.4
 - SDIO Host Specification version 2.00
 - 1-bit, 4-bit, 8-bit (MMC only) DAT bus width
 - SD cards with UHS-I interface compliant
 - Single Data Rate and Dual Data Rate modes
- ◆ Multislot operation
 - Configurable number of slots (1–4)
 - Independent clock/configuration for each slot
 - Data path (including DMA and FIFO) shared between all slots to reduce the silicon area
- ◆ Independent Interrupt and Wakeup outputs
- ◆ Integrated DMA controller
 - Optional, can be removed to reduce silicon area
 - SDMA (Simple DMA) mode
 - ADMA (Advanced DMA) mode with descriptor-based architecture and arbitrary data buffer alignment
- ◆ Data buffering
 - Configurable 32-bit FIFO buffers
 - Dual-Buffer mode for optimized throughput
 - Dual-Port or Single-Port RAM support
- ◆ Optional CPRM (Content Protection for Recordable Media)
 - Cryptomeria Cipher C2 hardware implementation
 - AKE (Authentication and Key Exchange)
- ◆ Low power features
 - Master SD card side clock can be switched off
 - Each card clock can be switched off independently
 - DP RAM can be replaced by SP RAM to reduce power
- ◆ Various System Interface options
 - Generic 8/16/32-bit master/slave interface
 - OCP 8/16/32-bit master/slave interface
 - AMBA AHB™ 32-bit master/slave interface

Implementation Results

Device		1-slot		1-slot, SDMA		1-slot, SDMA+ADMA		4-slot, SDMA+ADMA		
		Area	Speed	Area	Speed	Area	Speed	Area	Speed	
ALTERA	Stratix III	EP3S50-C3	3201 ALUTs 5 M9Ks	200MHz	4488 ALUTs 5 M9Ks	200MHz	5223 ALUTs 5 M9Ks	145Mhz	7056 ALUTs 8 M9Ks	145MHz
	Virtex-5		1512 SLICES 2 BRAM	200MHz	1859 SLICES 2 BRAM	200MHz	2151 SLICES 2 BRAM	111MHz	3530 SLICES 5 BRAM	111MHz
ASIC	TSMC 0.09um		33k gates	100 MHz	38k gates	100 MHz	45k gates	100 MHz	69k gates	100 MHz

Note: FIFO buffer size is 2 * 2kB for each configuration; 32-bit Generic interface; memories are implemented only in FPGA results; CPRM is not implemented.

Block Diagram



Functional Description

BIU – Bus Interface Unit

This module contains several subcomponents working in the clk system clock domain. It is responsible for communication with the host CPU. The Standard Register Set (SRS) slave interface provides the access to the internal register spaces, including Slot Register Set (SRS), Common Register Set (CRS), and proprietary Host Register Set (HRS). The DMA master interface can be provided as an option. It is possible to enable SDMA (Simple DMA) or ADMA (Advanced DMA) as defined by SDIO Host Specification version 2.0.

CIU – Card Interface Unit

This contains several subcomponents working in the sdmclk clock domain. CIU is responsible for communication with the SD/SDIO/MMC cards using the SD bus interface. It contains card clock dividers, Command/Response generation logic (CMD), and SD1/SD4/MMC 16-bit datapath logic (DAT). Most of the components are shared among all slots to reduce the area. Independent components for each slot are grouped in a Slot Control Unit (SCU). The optional CPRM module can be implemented for applications which require content encryption.

FIU – FIFO Interface Unit

This module implements the data buffer control logic used for data transactions. Two virtual buffers can be loaded inside the on-chip RAM. One of them is then dedicated to the BIU side, while the other can simultaneously be accessed by the CIU. Such assignment is called "dual-buffer" mode. The actual memory is implemented outside the core on the chip level. While DP-RAM memory can be used to achieve high performance (by enabling dual-buffer mode), SP-RAM (working in single-buffer mode only) aims at low power consumption and reduced silicon area.

SYN – Synchronization Logic

This provides the reliable cross clock domain synchronization for all control paths.

RSTC – Reset Controller

This generates the reset signal for every internal block of the SDIO-HOST. There are 4 reset triggers implemented inside the SDIO-HOST: hardware reset, software reset for all (clears all flip-flops except card detection logic), software reset for CMD (clears command/response logic), and software reset for DAT (clears the datapath logic).

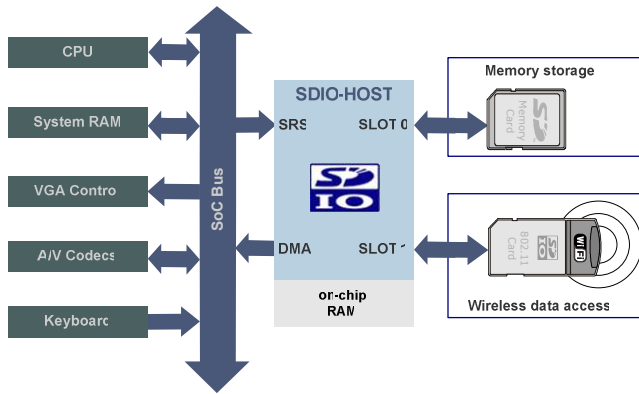
Pin Description

Name	Type	Polarity Bus Size	Description
Clock / Reset			
clk	in	rise	System clock
sdmclk	in	rise/fall	SD master clock
rst	in	high	Hardware Reset
Global Clock Control Signals			
ics	in	high	Clock Stable
ice	out	high	Clock Enable
Global Configuration Signals			
dualbuffer	in	high	Dual Buffer Enable
Common CPU-side Signals			
interrupt	out	High	Interrupt line
wakeup	out	High	Wakeup line
Card Slot Interfaces (separate signals per each slot)			
sdmclk_fb	in	1	Clock input
sdcd_n	in	1	Card detection
sdwp_n	in	1	Card write protect
cle	in	1	Current limit error
cmd_i	in	1	CMD line input
dat_i	in	16	DAT0 line input
psc_rdy	in	1	Input clock ready
sdclk	out	1	SD clock output
clkssel	out	1	SD clock select
led	out	1	LED on
bus_pow	out	1	SDIO power on
bus_volt	out	3	SD voltage select
bus_lvs	out	1	SD signaling level
cmd_o	out	2	CMD line output
dat0_o	out	16	DAT0 line output
cmd_en	out	2	CMD line enable
dat0_en	out	16	DAT0 line enable
psc_en	out	1	Clock input enable
psc_data	out	8	Clock input controller
DP/SP RAM Interface			
dualbuffer	in	high	Dual Buffer mode
biu_rdata	in	32	BIU read data
biu_we	out	high	BIU write enable
biu_re	out	high	BIU read enable
biu_addr	out	FIFODEPTH+1	BIU address
biu_wdata	out	32	BIU write data
ciu_rdata	in	32	CIU read data
ciu_we	out	high	CIU write enable
ciu_re	out	high	CIU read enable
ciu_addr	out	FIFODEPTH+1	CIU address
ciu_wdata	out	32	CIU write data

Name	Type	Polarity Bus Size	Description
SRS Generic Interface (Generic Interface version only)			
srs_req	in	high	SRS request
srs_rw	in	high	SRS read/write
srs_addr	in	11	SRS address
srs_be	in	SRSWIDTH/8	SRS byte enable
srs_wdata	in	SRSWIDTH	SRS write data
srs_ack	out	high	SRS acknowledge
srs_rdata	out	SRSWIDTH	SRS read data
DMA Generic Interface (Generic Interface version only)			
dma_ack	in	high	DMA acknowledge
dma_rdata	in	DMAWIDTH	DMA read data
dma_req	out	high	DMA request
dma_rw	out	high	DMA read/write
dma_eob	out	high	DMA end of burst
dma_addr	out	32	DMA address
dma_be	out	DMAWIDTH/8	DMA byte enable
dma_wdata	out	DMAWIDTH	DMA write data
SRS AHB Slave Interface (AMBA AHB™ version only)			
shsel	in	high	AHB selection
shaddr	in	11	AHB address
shtrans	in	2	AHB transfer type
shwrite	in	1	AHB direction
shsize	in	3	AHB transfer size
shburst	in	3	AHB burst type
shwdata	in	32	AHB write data
shready	out	high	AHB ready
shresp	out	2	AHB response
shrdata	out	32	AHB read data bus
DMA AHB Master Interface (AMBA AHB™ version only)			
mhgrant	in	high	AHB bus grant
mhready	in	high	AHB transfer done
mhresp	in	2	AHB response
mhrdata	in	32	AHB read data bus
mhbusreq	out	high	AHB bus request
mhlock	out	high	AHB locked
mhwrite	out	1	AHB direction
mhtrans	out	2	AHB transfer type
mhsize	out	3	AHB transfer size
mhbust	out	3	AHB burst type
mhprot	out	4	AHB protection
mhaddr	out	32	AHB bus address
mhwdata	out	32	AHB write data

Notes:

- SLOT_NUM, FIFODEPTH, SRSWIDTH, and DMAWIDTH are the generic parameters of the core. They can be customized by the user before synthesis.
- The interface option (Generic or AMBA AHB™) is to be specified by the user before ordering the core.



Example Application

The example application is a Personal Digital Assistant (PDA) design shown on the left, which is equipped with advanced audio-video and communication circuits. The Slot 0 of the SDIO-HOST Controller implemented inside the PDA provides access to external SD Memory cards, including SD High Capacity (SDHC) and Extended Capacity (SDXC) cards. The other slot of SDIO-HOST communicates with the wireless SDIO modem card. The software running on the CPU can implement such applications as a media player, a text processor, as well as a web browser and an e-mail client.

Configurability

The SDIO-HOST core can be configured by the user in order to meet requirements of target application and technology.

The following options can be changed before synthesis:

- ◆ Number of slots (1-4)
- ◆ Internal DMA (can be removed to reduce area). The following settings are possible:
 - DMA removed (register access only)
 - SDMA available
 - SDMA+ADMA available
- ◆ CPRM (can be enabled)
- ◆ FIFO Buffer size (512B – 2kB)
- ◆ Data bus width for Generic/OCP Interface

Additional parts of the system or modifications of the core can be developed by Evatronix, according to the user's requirements specific to his application. Please contact Evatronix directly to discuss any requests.

Options

The system bus can be selected among the following:

- ◆ 8/16/32-bit Generic Interface
- ◆ 8/16/32-bit OCP Interface
- ◆ 32-bit AMBA AHB™ Interface
- ◆ Other interface options are available on request

Additionally, the following options can be ordered:

- ◆ FPGA netlist files and place and route scripts
- ◆ OS-independent software driver
- ◆ Evaluation system, including:
 - EB-5 Tiny development board
 - Daughterboard, featuring 2 SD/MMC card slots
 - EB Programmer communication tool for PC
- ◆ Reference design for proprietary development board
- ◆ One-year maintenance
- ◆ On-site support and training

Standard Deliverables

- ◆ HDL source code for the SDIO-HOST
- ◆ Synthesis support (Synopsys) with a complete set of synthesis scripts
- ◆ Simulation support (Mentor Graphics, Cadence) with a set of scripts and macros
- ◆ Example SDIO-HOST-CHIP – a design which uses the SDIO-HOST and illustrates how to build and connect memories and tristate buffers
- ◆ Self-checking HDL Test Bench that instantiates:
 - Example design SDIO-HOST-CHIP
 - Bus Functional Models (Generic/OCP/AMBA AHB™)
 - SD Interface Bus Functional Models
 - SD Memory Card simulation model
 - SVA (System Verilog) SDIO protocol checker
- ◆ A collection of tests
- ◆ Comprehensive documentation including:
 - Design Specification with Programming section
 - Verification Specification with Test Plan
 - Integration Manual with User Guide

Related Products

SDIO-HOST Software Driver – a complete software packet that supports the SDIO-HOST Controller IP core. The driver allows a user to build applications without detailed knowledge of the SDIO Host controller hardware.

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